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## (54) High breakdown voltage semiconductor device

(57) A high breakdown voltage semiconductor device includes an active area (D1) and a surrounding region (D2). In the active area, a second semiconductor layer (2) of a second conductivity type is formed in a first semiconductor layer (1) of a first conductivity type. A third semiconductor layer (3) of the first conductivity type is formed in the second semiconductor layer. A gate electrode (6) faces through a gate insulating film the second semiconductor layer. A first main electrode (9) is connected to the second and third semiconductor layers. A ring layer (11) of the second conductivity type surrounds the active area at a position in the surrounding region. A first low-resistivity layer (13) is formed in the ring layer and has a resistivity lower than that of the ring layer. The first low-resistivity layer is connected to the first main electrode.

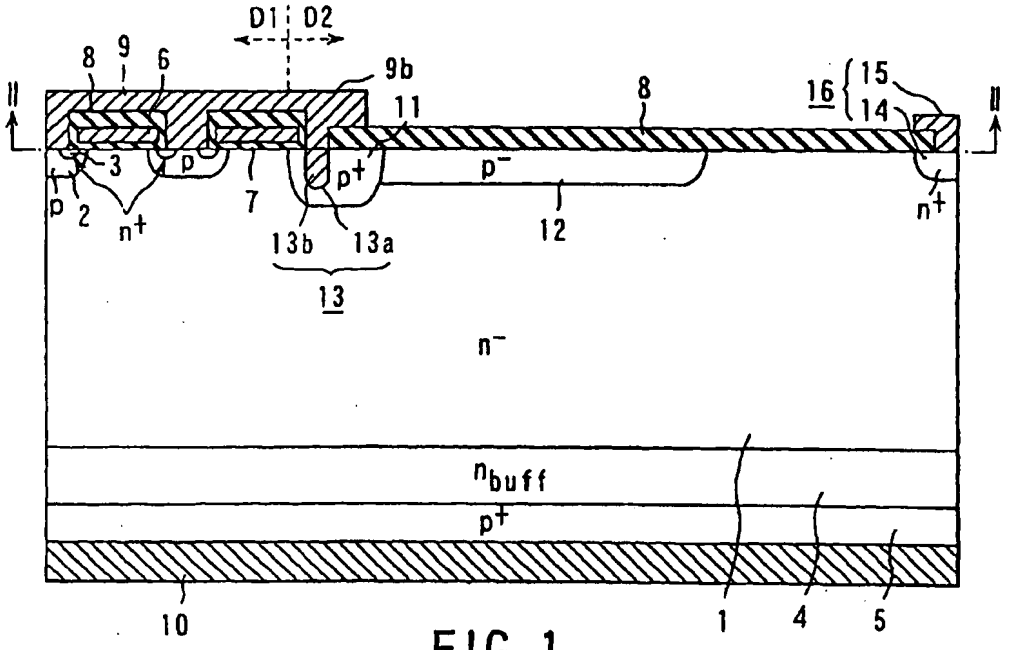



FIG. 1

EP 1 227 522 A2

## Description

**[0001]** The present invention relates to a high breakdown voltage semiconductor device having an insulated gate structure, such as an IGBT (Insulated Gate Bipolar Transistor), or a MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

**[0002]** An IGBT is a voltage-controlled device having both a high-speed switching characteristic like a MOSFET and a high power handling capability like a bipolar transistor. In recent years, IGBTs are widely used in power converters and switched mode power supplies in the power electronics field.

**[0003]** An explanation will be given of the structure of a conventional IGBT, taking a vertical type n-channel IGBT as an example, with reference to FIGS. 23 and 24. In general, arrays of IGBT unit cells are disposed in stripes in the central area (corresponding to an active area) other than the peripheral region (corresponding to a junction-termination region) on a semiconductor substrate. For the sake of simplicity, the IGBT will be partly explained, focusing on necessary portions.

**[0004]** FIG. 23 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of a conventional IGBT. FIG. 24 is a plan view taken along line XXIV - XXIV in FIG. 23.

**[0005]** As shown in FIG. 23, p-base layers 102 are formed by diffusion in the surface of an $n^-$-base layer 101. $N^+$-emitter layers 103 are formed by diffusion in the surfaces of the p-base layers 102. A gate electrode 106 is formed through a gate insulating film 107 on each of the portions of the p-base layers 102 between the $n^-$-base layer 101 and the $n^+$-emitter layers 103. An emitter electrode 109 is disposed in ohmic-contact with the $n^+$-emitter layers 103 and the p-base layers 102. A $p^+$-emitter layer 105 is formed through an n-buffer layer 104 on the bottom side of the $n^-$-base layer 101. A collector electrode 110 is disposed in ohmic-contact with the $p^+$-emitter layer 105.

**[0006]** As shown in FIG. 24, a $p^+$-ring layer 111 is formed in the junction-termination region and surrounds the central area (the active area) in which the arrays of IGBT unit cells are formed. The $p^+$-ring layer 111 is electrically connected to the emitter electrode 109 through a connection electrode 109b, which is integral with the emitter electrode 109. A ring-like $n^+$-diffusion layer 114 is formed in the junction-termination region, along the peripheral edge thereof. A ring-like stopper electrode 115 in an electrically floating state is disposed on the $n^+$-diffusion layer 114. The $n^+$-diffusion layer 114 and the stopper electrode 115 constitute an equi-potential ring 116. A $p^-$-RESURF (Reduced Surface Field) layer 112 is formed between the $p^+$-ring layer 111 and the $n^+$-diffusion layer 114 and in contact with the $p^+$-ring layer 111. The surface of the $n^-$-base layer 101 from the $p^+$-ring layer 111 to the $n^+$-diffusion layer 114 is covered with an insulating protection film 108.

**[0007]** When the IGBT is turned on, the following operation is performed. Specifically, while a positive bias is applied between the collector electrode 110 and the emitter electrode 109 (the plus is on the collector electrode 110 side), a positive voltage (a positive bias) relative to the emitter electrode 109 is applied to the gate electrodes 106. By doing so, n-inversion layers (not shown) are formed near the interfaces between the p-base layers 102 and the gate insulating films 107, and thus electrons are injected from the $n^+$-emitter layers 103 into the $n^-$-base layer 101. In accordance with the injection amount of the electrons, holes are injected from the $p^+$-emitter layer 105 into the $n^-$-base layer 101. As a result, the $n^-$-base layer 101 is filled with carriers and causes a conductivity modulation, and thus the resistance of the $n^-$-base layer 101 decreases to bring the IGBT into an ON-state.

**[0008]** On the other hand, when the IGBT is turned off, the following operation is performed. Specifically, in the ON-state described above, a negative bias is applied to the gate electrodes 106. By doing so, the n-inversion layers near the interfaces between the p-base layers 102 and the gate insulating films 107 disappear, and thus electrons stop being injected from the $n^+$-emitter layers 103 into the $n^-$-base layer 101. As a result, holes also stop being injected from the $p^+$-emitter layer 105 into the $n^-$-base layer 101. Then, carriers filling the $n^-$-base layer 101 are exhausted, and depletion layers expand from the junctions between the p-base layers 102 and the $n^-$-base layer 101 to bring the IGBT into an OFF-state.

**[0009]** During the turn-off operation, holes accumulated in the $n^-$-base layer 101 are exhausted through the p-base layers 102 into the emitter electrode 109, and through the $p^+$-ring layer 111 and the connection electrode 109b into the emitter electrode 109. In general, the $p^+$-ring layer 111 has a considerably large surface area, and a hole current concentrates at the contacting portion of the $p^+$-ring layer 111 with the connection electrode 109b. An excessive part of the hole current, which has not been allowed to flow through the contacting portion, mainly flows through the adjacent p-base layers 102. This current concentration gives rise to an increase in the potential of the p-base layers 102, and occasionally cause it to go beyond the junction potential (which is generally about 0.7V) between the p-base layers 102 and the $n^+$-emitter layers 103. In this case, the device falls in a latched-up state where electrons are directly injected from the $n^+$-emitter layers 103 into the $n^-$-base layer 101. As a result, electric current concentrates at the latched-up portion, thereby bringing about a thermal breakdown of the IGBT.

**[0010]** According to a first aspect of the present invention, there is provided a high breakdown voltage semiconductor device including an active area, and a surrounding region surrounding the active area, comprising:

a first semiconductor layer of a first conductivity

type disposed as a semiconductor active layer common to the active area and the surrounding region, the first semiconductor layer having first and second main surfaces opposite to each other;
a second semiconductor layer of a second conductivity type formed in the first main surface of the first semiconductor layer in the active area;
a third semiconductor layer of the first conductivity type formed in a surface of the second semiconductor layer;
a fourth semiconductor layer disposed on or in the second main surface of the first semiconductor layer in the active area;
a gate electrode facing, through a gate insulating film, a portion of the second semiconductor layer between the first semiconductor layer and the third semiconductor layer;
a first main electrode electrically connected to the second semiconductor layer and the third semiconductor layer;
a second main electrode electrically connected to the fourth semiconductor layer;
a ring layer of the second conductivity type formed in the first main surface of the first semiconductor layer and surrounding the active area at a position in the surrounding region adjacent to the active area;
a first low-resistivity layer formed in a surface of the ring layer and having a resistivity lower than that of the ring layer; and
a connection electrode electrically connecting the first low-resistivity layer to the first main electrode.

**[0011]** According to a second aspect of the present invention, there is provided a high breakdown voltage semiconductor device including an active area, and a junction-termination region surrounding the active area, comprising:

a first semiconductor layer of a first conductivity type disposed as a semiconductor active layer common to the active area and the junction-termination region, the first semiconductor layer having first and second main surfaces opposite to each other;
a second semiconductor layer of a second conductivity type formed in the first main surface of the first semiconductor layer in the active area;
a third semiconductor layer of the first conductivity type formed in a surface of the second semiconductor layer;
a fourth semiconductor layer disposed on or in the second main surface of the first semiconductor layer in the active area;
a gate electrode facing, through a gate insulating film, a portion of the second semiconductor layer between the first semiconductor layer and the third semiconductor layer;
a first main electrode electrically connected to the second semiconductor layer and the third semiconductor layer;
a second main electrode electrically connected to the fourth semiconductor layer;
a ring layer of the second conductivity type formed in the first main surface of the first semiconductor layer and surrounding the active area at a position in the junction-termination region adjacent to the active area;
a first low-resistivity layer formed in a surface of the ring layer and having a resistivity lower than that of the ring layer;
a connection electrode electrically connecting the first low-resistivity layer to the first main electrode
a second low-resistivity layer formed in a surface of the second semiconductor layer and having a resistivity lower than that of the second semiconductor layer, the second low-resistivity layer being disposed in contact with the first main electrode and the second and third semiconductor layers, the second low-resistivity layer consisting essentially of a material the same as that of the first low-resistivity layer;
an end layer of the first conductivity type formed in the first main surface of the first semiconductor layer along a peripheral edge of the first semiconductor layer in the junction-termination region, the end layer having a carrier impurity concentration higher than that of the first semiconductor layer; and
a third low-resistivity layer formed in a surface of the end layer and having a resistivity lower than that of the end layer, the third low-resistivity layer consisting essentially of a material the same as that of the first low-resistivity layer.

**[0012]** This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

**[0013]** The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a first embodiment of the present invention;
FIG. 2 is a plan view taken along line II - II in FIG. 1;
FIG. 3 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a second embodiment of the present invention;
FIG. 4 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a third embodiment of the present invention;
FIG. 5 is a sectional view schematically showing the junction-termination region and a portion of the ac-

tive area near there, of an IGBT according to a fourth embodiment of the present invention;
FIG. 6 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fifth embodiment of the present invention;
FIG. 7 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a sixth embodiment of the present invention;
FIG. 8 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a seventh embodiment of the present invention;
FIG. 9 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to an eighth embodiment of the present invention;
FIG. 10 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a ninth embodiment of the present invention;
FIG. 11 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a tenth embodiment of the present invention;
FIG. 12 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to an eleventh embodiment of the present invention;
FIG. 13 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a twelfth embodiment of the present invention;
FIG. 14 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a thirteenth embodiment of the present invention;
FIG. 15 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fourteenth embodiment of the present invention;
FIG. 16 is a plan view taken along line XVI - XVI in FIG. 15;
FIG. 17 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fifteenth embodiment of the present invention;
FIG. 18 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a sixteenth embodiment of the present invention;
FIG. 19 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a seventeenth embodiment of the present invention;
FIG. 20 is a sectional view schematically showing the active area of an IGBT according to an eighteenth embodiment of the present invention;
FIG. 21 is a plan view taken along line XXI - XXI in FIG. 20;
FIG. 22 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of a power MOSFET according to a nineteenth embodiment of the present invention;
FIG. 23 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of a conventional IGBT; and
FIG. 24 is a plan view taken along line XXIV - XXIV in FIG. 23.

**[0014]** Embodiments of the present invention will be described hereinafter with reference to the accompanying drawings. In the following description, the constituent elements having substantially the same function and arrangement are denoted by the same reference numerals, and a repetitive description will be made only when necessary.

**[0015]** In general, a high breakdown voltage semiconductor device has arrays of device unit cells, which are disposed in stripes, in the central area (corresponding to an active area) other than the peripheral region (corresponding to a junction-termination region) on a semiconductor substrate. In the following embodiments, for the sake of simplicity, the device will be partly explained, focusing on necessary portions. Furthermore, in the following description, the first conductivity type will be the n-type, while the second conductivity type will be the p-type.

(First Embodiment)

**[0016]** FIG. 1 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a first embodiment of the present invention. FIG. 2 is a plan view taken along line II - II in FIG. 1.

**[0017]** As shown in FIG. 1, an $n^-$-base layer (a first base layer) 1 is disposed as a semiconductor active layer common to the central area (corresponding to an active area) D1, in which arrays of IGBT unit cells are disposed, and the peripheral region (corresponding to a junction-termination region) D2 surrounding the central area. The $n^-$-base layer 1 has a first main surface (the top side) and a second main surface (the bottom side) opposite to each other. A plurality of p-base layers (second base layers) 2 are selectively formed in stripes by diffusion in the central area on the top side of the $n^-$-base layer 1.

**[0018]** Two $n^+$-emitter layers (first emitter layers) 3 are selectively formed in stripes by diffusion in each of the p-base layers 2. A gate electrode 6 is formed through a gate insulating film 7 on the portion between one of the $n^+$-emitter layers 3 in one of each pair of two p-base layers 2, which are adjacent to each other, and one of the

$n^+$-emitter layers 3 in the other of the two p-base layers 2. A gate electrode 6 is also formed through a gate insulating film 7 on the portion between one of the $n^+$-emitter layers 3 in each outermost p-base layer 2 and a $p^+$-ring layer 11 described later.

**[0019]** An emitter electrode (a first main electrode) 9 is disposed in ohmic-contact with the p-base layers 2 and the $n^+$-emitter layers 3 at respective positions on the p-base layers 2. The emitter electrode 9 is disposed on the gate electrodes 6 through an insulating protection film 8. A $p^+$-emitter layer (a second emitter layer) 5 is formed through an n-buffer layer 4 on the bottom side of the $n^-$-base layer 1. A collector electrode (a second main electrode) 10 is disposed in ohmic-contact with the $p^+$-emitter layer 5.

**[0020]** As shown in FIG. 2, a $p^+$-ring layer 11 is formed in the junction-termination region D2 and surrounds the central area (the active area) D1 in which the arrays S of IGBT unit cells are formed. The $p^+$-ring layer 11 is electrically connected to the emitter electrode 9 through a connection electrode 9b, which is integral with the emitter electrode 9.

**[0021]** A ring-like $n^+$-diffusion layer 14 is formed in the junction-termination region, along the peripheral edge thereof. The $n^+$-diffusion layer 14 is of a conductivity type the same as that of the $n^-$-base layer 1 and has a carrier impurity concentration higher than that of the $n^-$-base layer 1. A ring-like stopper electrode 15 in an electrically floating state is disposed on the $n^+$-diffusion layer 14. The $n^+$-diffusion layer 14 and the stopper electrode 15 constitute an equi-potential ring 16.

**[0022]** The surface of the $n^-$-base layer 1 from the $p^+$-ring layer 11 to the $n^+$-diffusion layer 14 is covered with an insulating protection film 8. A $p^-$-RESURF layer 12 is formed in the surface of the $n^-$-base layer 1, disposed in contact with the $p^+$-ring layer 11, and extends under the protection film 8 in the junction-termination region. The $p^-$-RESURF layer 12 is of a conductivity type the same as that of the $p^+$-ring layer 11 and has a carrier impurity concentration lower than that of $p^+$-ring layer 11.

**[0023]** A ring-like low-resistivity layer 13 having a resistivity lower than that of the $p^+$-ring layer 11 is formed in the surface of the layer 11.

The low-resistivity layer 13 has a resistivity of from $1 \times 10^{-6}$ to $1 \times 10^{-3}$ Ω·cm and a depth of from 0.5 to 8 μm. The low-resistivity layer 13 is disposed on the active area side relative to the center of the $p^+$-ring layer 11. The low-resistivity layer 13 is electrically connected to the emitter electrode 9 through the connection electrode 9b, which is integral with the emitter electrode 9. The low-resistivity layer 13 is made of a conductive material 13b buried in a trench 13a formed in the $p^+$-ring layer 11.

**[0024]** As the conductive material 13b of the low-resistivity layer 13, a metal the same as that of the emitter electrode 9 and the connection electrode 9b, such as aluminum (Al) used in general, is preferably used, because its contact resistance with the emitter electrode is negligible. Where the conductive material 13b is the same as the material of the emitter electrode 9, the low-resistivity layer 13 can be formed along with the emitter electrode 9 in the same step by patterning a conductive film common to the emitter electrode 9. On the other hand, where it is necessary to consider a thermal treatment to be performed in a later step, a refractory metal, such as Mo, Ti, or W, is preferably used as the conductive material 13b. Furthermore, the conductive material 13b may consist of a semiconductor, such as polycrystalline silicon, which is of a conductivity type the same as that of the $p^+$-ring layer 11 and has a carrier impurity concentration higher than that of $p^+$-ring layer 11.

**[0025]** The low-resistivity layer 13 is disposed close to the pn junction between the $n^-$-base layer 1 and the $p^+$-ring layer 11. With this arrangement, a hole current concentrating at the $p^+$-ring layer 11 is allowed to swiftly flow into the emitter electrode 9. The low-resistivity layer 13 is partially disposed on the p-base layers 2 side relative to the center of the $p^+$-ring layer 11. With this arrangement, a smaller amount of hole current is allowed to flow into the p-base layers 2.

**[0026]** When the IGBT is turned on, the following operation is performed. Specifically, while a positive bias is applied between the collector electrode 10 and the emitter electrode 9 (the plus is on the collector electrode 10 side), a positive voltage (a positive bias) relative to the emitter electrode 9 is applied to the gate electrodes 6. By doing so, n-inversion layers (not shown) are formed near the interfaces between the p-base layers 2 and the gate insulating films 7, and thus electrons are injected from the $n^+$-emitter layers 3 into the $n^-$-base layer 1. In accordance with the injection amount of the electrons, holes are injected from the $p^+$-emitter layer 5 into the $n^-$-base layer 1. As a result, the $n^-$-base layer 1 is filled with carriers and causes a conductivity modulation, and thus the resistance of the $n^-$-base layer 1 decreases to bring the IGBT into an ON-state.

**[0027]** On the other hand, when the IGBT is turned off, the following operation is performed. Specifically, in the ON-state described above, a negative bias is applied to the gate electrodes 6. By doing so, the n-inversion layers near the interfaces between the p-base layers 2 and the gate insulating films 7 disappear, and thus electrons stop being injected from the $n^+$-emitter layers 3 into the $n^-$-base layer 1. As a result, holes also stop being injected from the $p^+$-emitter layer 5 into the $n^-$-base layer 1. Then, carriers filling the $n^-$-base layer 1 are exhausted, and depletion layers expand from the junctions between the p-base layers 2 and the $n^-$-base layer 1 to bring the IGBT into an OFF-state.

**[0028]** During the turn-off operation, holes accumulated in the $n^-$-base layer 1 are exhausted through the $p^+$-ring layer 11, the low-resistivity layer 13, and the connection electrode 9b into the emitter electrode 9, and through the p-base layers 2 into the emitter electrode 9. Since the low-resistivity layer 13 formed in the $p^+$-ring layer 11 allows holes to easily flow, a hole current con-

centrates at the $p^+$-ring layer 11 preferentially to the adjacent p-base layers 2. Consequently, the adjacent p-base layers 2 are prevented from increasing the potential, thereby improving the withstanding property of the IGBT against breakdown.

**[0029]** The distance from the pn junction between the $p^+$-ring layer 11 and the $n^-$-base layer 1 to the low-resistivity layer 13 is set to be a distance at which a depletion layer extends from the pn junction into the $p^+$-ring layer 11 when the IGBT is statically withstanding in an OFF-state. With this arrangement, the low-resistivity layer 13 can be utilized as a protection mechanism when the IGBT is supplied with an excessive voltage.

(Second Embodiment)

**[0030]** FIG. 3 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a second embodiment of the present invention.

**[0031]** In this embodiment, the structure of the first embodiment is modified such that a ring-like low-resistivity layer 26 having a resistivity lower than that of an $n^+$-diffusion layer 14 is formed in the surface of the layer 14. The low-resistivity layer 26 is disposed in a trench 25 formed in the $n^+$-diffusion layer 14. The trench 25 may have a depth substantially the same as that of a trench 13a formed in a $p^+$-ring layer 11. The low-resistivity layer 26 is electrically connected to a stopper electrode 15. The low-resistivity layer 26 functions to stabilize the potential of the $n^+$-diffusion layer 14.

**[0032]** Similarly to a low-resistivity layer 13 in the $p^+$-ring layer 11, the low-resistivity layer 26 is made of an ordinary wiring metal, a refractory metal, or a semiconductor. Where the low-resistivity layer 26 is formed along with the low-resistivity layer 13 in the same step, the number of manufacturing steps is prevented from increasing. In this case, the low-resistivity layer 26 is made of a material substantially the same as that of the low-resistivity layer 13. Particularly, where the low-resistivity layer 26, as well as the low-resistivity layer 13, is made of a material the same as that of the emitter electrode 9, the low-resistivity layer 26, as well as the low-resistivity layer 13, can be formed along with the emitter electrode 9 in the same step by patterning a conductive film common to the emitter electrode 9.

(Third Embodiment)

**[0033]** FIG. 4 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a third embodiment of the present invention.

**[0034]** In this embodiment, the structure of the second embodiment is modified such that a low-resistivity layer 26 penetrates an $n^+$-diffusion layer 14 and extends into an $n^-$-base layer 1. In this case, the low-resistivity layer 26 prevents depletion layers from expanding to the outside of the $n^+$-diffusion layer 14, when the depletion layers expand from the junctions between p-base layers 2 and the $n^-$-base layer 1 and reach the $n^+$-diffusion layer 14 in an OFF-state of IGBT. As a result, the breakdown voltage of the IGBT is improved. Furthermore, since the $n^+$-emitter layers 3 and the $n^+$-diffusion layer 14 can be formed at the same time, the number of manufacturing steps is prevented from increasing. The relationship between the $n^+$-diffusion layer 14 and the low-resistivity layer 26 shown in FIG. 4 is applicable to the following embodiments in the same manner.

(Fourth Embodiment)

**[0035]** FIG. 5 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fourth embodiment of the present invention.

**[0036]** In this embodiment, the structure of the first embodiment is modified such that a conductive field plate 17 is used in place of the $p^-$-RESURF layer 12. The field plate 17 extends on top of a protection film 8 in the junction-termination region. The field plate 17 is electrically connected to a low-resistivity layer 13 and an emitter electrode 9.

**[0037]** Also in this embodiment, the low-resistivity layer 13 formed in a $p^+$-ring layer 11 improves the withstanding property of the IGBT against breakdown. The field plate 17 functions to laterally expand an equi-potential plane in an OFF-state, thereby relaxing electrical field concentration to improve the breakdown voltage.

(Fifth Embodiment)

**[0038]** FIG. 6 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fifth embodiment of the present invention.

**[0039]** In this embodiment, the structure of the fourth embodiment is modified such that a ring-like low-resistivity layer 26 having a resistivity lower than that of an $n^+$-diffusion layer 14 is formed in the surface of the layer 14. The low-resistivity layer 26 is disposed in a trench 25 formed in the $n^+$-diffusion layer 14. The low-resistivity layer 26 is electrically connected to a stopper electrode 15. The function and manufacturing method of the low-resistivity layer 26 have been explained with reference to FIG. 3.

(Sixth Embodiment)

**[0040]** FIG. 7 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a sixth embodiment of the present invention.

**[0041]** In this embodiment, the structure of the first embodiment is modified such that a plurality of $p^+$-guard ring layers 18 are used in place of the $p^-$-RESURF layer

12. The $p^+$-guard ring layers 18 are formed in the surface of an $n^-$-base layer 1 between a $p^+$-ring layer 11 and an $n^+$-diffusion layer 14. The $p^+$-guard ring layers 18 are of a conductivity type the same as that of the $p^+$-ring layer 11 and have a carrier impurity concentration higher than that of the $p^+$-ring layer 11. The distances between the $p^+$-guard ring layers 18 become gradually larger toward the peripheral edge.

**[0042]** Also in this embodiment, a low-resistivity layer 13 formed in the $p^+$-ring layer 11 improves the withstanding property of the IGBT against breakdown. The $p^+$-guard ring layers 18 cause the potential to gradually increase from the $p^+$-ring layer 11 to an equi-potential ring 16 in an OFF-state of the IGBT. In other words, the $p^+$-guard ring layers 18 function to laterally expand an equi-potential plane in an OFF-state, thereby relaxing electrical field concentration to improve the breakdown voltage. The breakdown voltage can be controlled by changing the number of the $p^+$-guard ring layers 18.

(Seventh Embodiment)

**[0043]** FIG. 8 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a seventh embodiment of the present invention.

**[0044]** In this embodiment, the structure of the sixth embodiment is modified such that a ring-like low-resistivity layer 26 having a resistivity lower than that of an $n^+$-diffusion layer 14 is formed in the surface of the layer 14. The low-resistivity layer 26 is disposed in a trench 25 formed in the $n^+$-diffusion layer 14. The low-resistivity layer 26 is electrically connected to a stopper electrode 15. The function and manufacturing method of the low-resistivity layer 26 have been explained with reference to FIG. 3.

**[0045]** Also, ring-like low-resistivity layers 28 having a resistivity lower than that of $p^+$-guard ring layers 18 are respectively formed in the surfaces of the layers 18. The low-resistivity layers 28 are disposed in trenches 27 formed in the $p^+$-guard ring layers 18. The trenches 27 may have a depth substantially the same as that of a trench 13a formed in a $p^+$-ring layer 11. The low-resistivity layers 28 are electrically connected to guard ring electrodes 29 disposed thereon in an electrically floating state. The guard ring electrodes 29 and the low-resistivity layers 28 function to stabilize the potentials of the $p^+$-guard ring layers 18.

**[0046]** Similarly to a low-resistivity layer 13 in the $p^+$-ring layer 11, the low-resistivity layers 28 are made of an ordinary wiring metal, a refractory metal, or a semiconductor. Where the low-resistivity layers 28 are formed along with the low-resistivity layer 13 in the same step, the number of manufacturing steps is prevented from increasing. In this case, the low-resistivity layers 28 are made of a material substantially the same as that of the low-resistivity layer 13. Particularly, where the guard ring electrodes 29 and the low-resistivity layers 28, as well as the low-resistivity layers 13 and 26, are made of a material the same as that of the emitter electrode 9, the guard ring electrodes 29 and the low-resistivity layers 28, as well as the low-resistivity layers 13 and 26, can be formed along with the emitter electrode 9 in the same step by patterning a conductive film common to the emitter electrode 9.

(Eighth Embodiment)

**[0047]** FIG. 9 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to an eighth embodiment of the present invention.

**[0048]** In this embodiment, the structure of the sixth embodiment is modified such that a protection film 19 made of a semi-insulating material (a high resistivity material) is formed in place of the protection film (an oxide film) 8 made of an insulating material. The protection film 19 consists of, e.g., SIPOS (Semi-Insulating Polycrystalline Silicon).

**[0049]** Also in this embodiment, a low-resistivity layer 13 formed in a $p^+$-ring layer 11 improves the withstanding property of the IGBT against breakdown. The protection film 19 makes the device less sensitive to the influence of electrical charges outside the IGBT, thereby preventing the breakdown voltage of the IGBT from lowering.

(Ninth Embodiment)

**[0050]** FIG. 10 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a ninth embodiment of the present invention.

**[0051]** In this embodiment, the structure of the sixth embodiment is modified such that ring-like low-resistivity layers 24 having a resistivity lower than that of p-base layers 2 are respectively formed in the surfaces of the layers 2. The low-resistivity layers 24 are disposed in trenches 23 formed in the p-base layers 2. The low-resistivity layers 24 are disposed in contact with an emitter electrode 9, the p-base layers 2, and $n^+$-emitter layers 3. A trench 20 is formed above a low-resistivity layer 13 in a $p^+$-ring layer 11. The trenches 20 and 23 are formed by etching to have a depth of, e.g., about 1.0 μm.

**[0052]** Similarly to the low-resistivity layer 13 in the $p^+$-ring layer 11, the low-resistivity layers 24 are made of an ordinary wiring metal, a refractory metal, or a semiconductor. Where the low-resistivity layers 24 are formed along with the low-resistivity layer 13 in the same step, the number of manufacturing steps is prevented from increasing. In this case, the low-resistivity layers 24 are made of a material substantially the same as that of the low-resistivity layer 13. Particularly, where the low-resistivity layers 24, as well as the low-resistivity layer 13, are made of a material the same as that of the emitter electrode 9, the low-resistivity layers 24, as well

as the low-resistivity layer 13, can be formed along with the emitter electrode 9 in the same step by patterning a conductive film common to the emitter electrode 9.

**[0053]** Also in this embodiment, the low-resistivity layer 13 formed in the $p^+$-ring layer 11 improves the withstanding property of the IGBT against breakdown. The p-base layers 2 are connected to the emitter electrode 9 through the low-resistivity layers 24 disposed in the trenches 23, thereby improving the contacting property. In addition, since the distance between an $n^-$-base layer 1 and the emitter electrode 9 is reduced and the lateral resistance of the p-base layers 2 decreases, the current value at which a latched-up state is brought about is raised. In other words, this arrangement further improves the withstanding property against a latched-up state.

(Tenth Embodiment)

**[0054]** FIG. 11 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a tenth embodiment of the present invention.

**[0055]** In this embodiment, the structure of the ninth embodiment is modified such that a ring-like low-resistivity layer 26 having a resistivity lower than that of an $n^+$-diffusion layer 14 is formed in the surface of the layer 14. The low-resistivity layer 26 is disposed in a trench 25 formed in the $n^+$-diffusion layer 14. The low-resistivity layer 26 is electrically connected to a stopper electrode 15. The function and manufacturing method of the low-resistivity layer 26 have been explained with reference to FIG. 3.

**[0056]** Also, ring-like low-resistivity layers 28 having a resistivity lower than that of $p^+$-guard ring layers 18 are respectively formed in the surfaces of the layers 18. The low-resistivity layers 28 are disposed in trenches 27 formed in the $p^+$-guard ring layers 18. The low-resistivity layers 28 are electrically connected to guard ring electrodes 29 disposed thereon in an electrically floating state. The function and manufacturing method of the low-resistivity layers 28 have been explained with reference to FIG. 8.

**[0057]** A low-resistivity layer 13 formed in a $p^+$-ring layer 11, low-resistivity layers 24 formed in p-base layers 2, the low-resistivity layer 26 formed in the $n^+$-diffusion layer 14, and the low-resistivity layers 28 formed in the $p^+$-guard ring layers 18 are made of substantially the same material. Particularly, where the low-resistivity layers 13, 24, 26, and 28 are made of a material the same as that of the emitter electrode 9, these low-resistivity layers can be formed along with the emitter electrode 9 in the same step by patterning a conductive film common to the emitter electrode 9. The trenches 13a, 23, 25, and 27 accommodating the low-resistivity layers 13, 24, 26, and 28 may have substantially the same depth.

(Eleventh Embodiment)

**[0058]** FIG. 12 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to an eleventh embodiment of the present invention.

**[0059]** In this embodiment, the structure of the tenth embodiment is modified such that a $p^-$-RESURF layer 12 is formed in the surface of an $n^-$-base layer 1 in place of the $p^+$-guard ring layers 18. The $p^-$-RESURF layer 12 is formed in contact with a $p^+$-ring layer 11 and extends under the protection film 8 in the junction-termination region. The $p^-$-RESURF layer 12 functions to laterally expand an equi-potential plane in an OFF-state, thereby relaxing electrical field concentration to improve the breakdown voltage.

(Twelfth Embodiment)

**[0060]** FIG. 13 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a twelfth embodiment of the present invention.

**[0061]** In this embodiment, the structure of the tenth embodiment is modified such that a conductive field plate 17 is used in place of the $p^+$-guard ring layers 18. The field plate 17 extends on top of a protection film 8 in the junction-termination region. The field plate 17 is electrically connected to a low-resistivity layer 13 and an emitter electrode 9. The field plate 17 functions to laterally expand an equi-potential plane in an OFF-state, thereby relaxing electrical field concentration to improve the breakdown voltage.

(Thirteenth Embodiment)

**[0062]** FIG. 14 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a thirteenth embodiment of the present invention.

**[0063]** In this embodiment, the structure of the sixth embodiment is modified such that each of gate insulating films 21 is formed of first and second portions 21a and 21b having thicknesses different from each other. The first portions 21a of each gate insulating film 21 have a smaller thickness and are located on the portions of the corresponding p-base layer 2 (the channel region) between an $n^-$-base layer 1 and the $n^+$-emitter layers 3. The other portion of each gate insulating film 21 (the second portion 21b) has a larger thickness.

**[0064]** Also in this embodiment, a low-resistivity layer 13 formed in a $p^+$-ring layer 11 improves the withstanding property of the IGBT against breakdown. Since each gate insulating film 21 has a large thickness at a portion other than the channel region, the capacitance between the gate and the collector decreases. Consequently, the IGBT can operate more uniformly at a higher speed. The structure of the gate insulating films 21 is applicable to

the first to twelfth embodiments described above, and eighteenth and nineteenth embodiments described later.

(Fourteenth Embodiment)

[0065] FIG. 15 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fourteenth embodiment of the present invention. FIG. 16 is a plan view taken along line XVI - XVI in FIG. 15. This IGBT has a structure of the trench gate type.

[0066] As shown in FIG. 15, an $n^-$-base layer (a first base layer) 31 is disposed as a semiconductor active layer common to the central area (corresponding to an active area) D1, in which arrays of IGBT unit cells are disposed, and the peripheral region (corresponding to a junction-termination region) D2 surrounding the central area. The $n^-$-base layer 31 has a first main surface (the top side) and a second main surface (the bottom side) opposite to each other. A plurality of p-base layers (second base layers) 32 are selectively formed in stripes by diffusion in the central area on the top side of the $n^-$-base layer 31.

[0067] A plurality of trenches 45 are formed in the $n^-$-base layer 31 and the p-base layers 32, such that they penetrate the p-base layers 32 and extend into the $n^-$-base layer 31 halfway. A gate electrode 46 is formed and buried through a gate insulating film 47 in each of the trenches 45. The combination of the trench 45, the gate insulating film 47, and the gate electrode 46 constitutes a trench gate 44. $N^+$-emitter layers (first emitter layers) 33 are selectively formed in contact with sides of the trench gates 44 by diffusion in the surfaces of the p-base layers 32.

[0068] An emitter electrode (a first main electrode) 39 is disposed in ohmic-contact with the p-base layers 32 and the $n^+$-emitter layers 33 at respective positions in the gaps between the trench gates 44. The emitter electrode 39 is disposed on the gate electrodes 46 through an insulating protection film 38. A $p^+$-emitter layer (a second emitter layer) 35 is formed through an n-buffer layer 34 on the bottom side of the $n^-$-base layer 31. A collector electrode (a second main electrode) 40 is disposed in ohmic-contact with the $p^+$-emitter layer 35.

[0069] As shown in FIG. 16, a $p^+$-ring layer 41 is formed in the junction-termination region D2 and surrounds the central area (the active area) D1 in which the arrays S of IGBT unit cells are formed. The $p^+$-ring layer 41 is disposed in contact with the outermost trench gates 44. The $p^+$-ring layer 41 is electrically connected to the emitter electrode 39 through a connection electrode 39b, which is integral with the emitter electrode 39.

[0070] A ring-like $n^+$-diffusion layer 54 is formed in the junction-termination region, along the peripheral edge thereof. The $n^+$-diffusion layer 54 is of a conductivity type the same as that of the $n^-$-base layer 31 and has a carrier impurity concentration higher than that of the $n^-$-base layer 31. A ring-like stopper electrode 55 in an electrically floating state is disposed on the $n^+$-diffusion layer 54. The $n^+$-diffusion layer 54 and the stopper electrode 55 constitute an equi-potential ring 56.

[0071] The surface of the $n^-$-base layer 31 from the $p^+$-ring layer 41 to the $n^+$-diffusion layer 54 is covered with an insulating protection film 38. A $p^-$-RESURF layer 42 is formed in the surface of the $n^-$-base layer 31, disposed in contact with the $p^+$-ring layer 41, and extends under the protection film 38 in the junction-termination region. The $p^-$-RESURF layer 42 is of a conductivity type the same as that of the $p^+$-ring layer 41 and has a carrier impurity concentration lower than that of $p^+$-ring layer 41.

[0072] A ring-like low-resistivity layer 43 having a resistivity lower than that of the $p^+$-ring layer 41 is formed in the surface of the layer 41. The low-resistivity layer 43 has a resistivity of from $1 \times 10^{-6}$ to $1 \times 10^{-3}$ Ω·cm and a depth of from 0.5 to 8 μm. The low-resistivity layer 43 is disposed on the active area side relative to the center of the $p^+$-ring layer 41. The low-resistivity layer 43 is electrically connected to the emitter electrode 39 through the connection electrode 39b, which is integral with the emitter electrode 39. The low-resistivity layer 43 is made of a conductive material 43b buried in a trench 43a formed in the $p^+$-ring layer 41.

[0073] As the conductive material 43b of the low-resistivity layer 43, a metal the same as that of the emitter electrode 39 and the connection electrode 39b, such as aluminum (Al) used in general, is preferably used, because its contact resistance with the emitter electrode is negligible. Where the conductive material 43b is the same as the material of the emitter electrode 39, the low-resistivity layer 43 can be formed along with the emitter electrode 39 in the same step by patterning a conductive film common to the emitter electrode 39. On the other hand, where it is necessary to consider a thermal treatment to be performed in a later step, a refractory metal, such as Mo, Ti, or W, is preferably used as the conductive material 43b. Furthermore, the conductive material 43b may consist of a semiconductor, such as polycrystalline silicon, which is of a conductivity type the same as that of the $p^+$-ring layer 41 and has a carrier impurity concentration higher than that of $p^+$-ring layer 41.

[0074] The low-resistivity layer 43 is disposed close to the pn junction between the $n^-$-base layer 31 and the $p^+$-ring layer 41. With this arrangement, a hole current concentrating at the $p^+$-ring layer 41 is allowed to swiftly flow into the emitter electrode 39. The low-resistivity layer 43 is partially disposed on the p-base layers 32 side relative to the center of the $p^+$-ring layer 41. With this arrangement, a smaller amount of hole current is allowed to flow into the p-base layers 32.

[0075] The operation of the IGBT of the trench gate type according to this embodiment is the same as that of the IGBT according to the first embodiment, and thus a description thereof will be omitted.

[0076] During the turn-off operation, holes accumulat-

ed in the n⁻-base layer 31 are exhausted through the p⁺-ring layer 41, the low-resistivity layer 43, and the connection electrode 39b into the emitter electrode 39, and through the p-base layers 32 into the emitter electrode 39. Since the low-resistivity layer 43 formed in the p⁺-ring layer 41 allows holes to easily flow, a hole current concentrates at the p⁺-ring layer 41 preferentially to the adjacent p-base layers 32. Consequently, the adjacent p-base layers 32 are prevented from increasing the potential, thereby improving the withstanding property of the IGBT against breakdown.

**[0077]** Where the intervals between trenches 45 are small, the gaps between the trenches 45 form current passageways narrow enough to increase resistance against the flow of holes from the n⁻-base layer 31 toward the emitter electrode 39 in an ON-state of the IGBT. With this arrangement, it is possible to increase the ability to inject electrons from n⁺-emitter layers 33 into the n⁻-base layer 31.

(Fifteenth Embodiment)

**[0078]** FIG. 17 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a fifteenth embodiment of the present invention;

**[0079]** In this embodiment, the structure of the fourteenth embodiment is modified such that a ring-like low-resistivity layer 26 having a resistivity lower than that of an n⁺-diffusion layer 54 is formed in the surface of the layer 54. The low-resistivity layer 26 is disposed in a trench 25 formed in the n⁺-diffusion layer 54. The low-resistivity layer 26 is electrically connected to a stopper electrode 55. The function and manufacturing method of the low-resistivity layer 26 have been explained with reference to FIG. 3.

**[0080]** Particularly, where the low-resistivity layer 26, as well as the low-resistivity layer 43, is made of a material the same as that of the emitter electrode 39, the low-resistivity layer 26, as well as the low-resistivity layer 43, can be formed along with the emitter electrode 39 in the same step by patterning a conductive film common to the emitter electrode 39. Furthermore, where the trenches 45, 43a, and 25 have substantially the same depth, they are easily formed at the same time.

(Sixteenth Embodiment)

**[0081]** FIG. 18 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a sixteenth embodiment of the present invention.

**[0082]** In this embodiment, the structure of the fifteenth embodiment is modified such that oxide films 43c and 57 are formed on the sidewalls in trenches 43a and 25. Even this arrangement provides effects the same as those of the fifteenth embodiment. The structure of this embodiment may be formed by the following method.

**[0083]** Specifically, when buried gate structures are formed in trenches 45, buried gate structures, each formed of an insulating oxide film and an electrode, are also formed in the trenches 43a and 25. Then, only the electrodes are removed from the buried gate structures in the trenches 43a and 25 to leave the insulating oxide films 43c and 57. Then, the portions of the insulating oxide films 43c and 57 at the bottom of trenches 43a and 25 are removed by an anisotropic etching. Then, when an emitter electrode 39 is formed, the electrode material is buried in the trenches 43a and 25.

(Seventeenth Embodiment)

**[0084]** FIG. 19 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of an IGBT according to a seventeenth embodiment of the present invention.

**[0085]** In this embodiment, the structure of the fourteenth embodiment is modified such that there are dummy gap portions 58, each of which is formed of a semiconductor layer portion between two trenches 45 and out of contact with an emitter electrode 39. The dummy gap portions 58 and current-passageway gap portions are alternately disposed. Not being limited to one dummy gap portion 58, two or more dummy gap portions 58 may be disposed between two current-passageway gap portions, which are adjacent to each other.

**[0086]** Also in this embodiment, a low-resistivity layer 43 formed in a p⁺-ring layer 41 improves the withstanding property of the IGBT against breakdown. In addition, the dummy gap portions 58 further increase resistance against the flow of holes from an n⁻-base layer 31 toward the emitter electrode 39 in an ON-state of the IGBT. With this arrangement, it is possible to further increase the ability to inject electrons from n⁺-emitter layers 33 into the n⁻-base layer 31.

(Eighteenth Embodiment)

**[0087]** FIG. 20 is a sectional view schematically showing the active area of an IGBT according to an eighteenth embodiment of the present invention. FIG. 21 is a plan view taken along line XXI - XXI in FIG. 20.

**[0088]** An IGBT having a large surface area may have emitter electrodes respectively allocated to divided areas and gate wirings disposed around the emitter electrodes, in order to prevent gate signal delays. An IGBT having such a structure is sometimes provided with a p⁺-ring layer under the gate wirings, thereby preventing the breakdown voltage from lowering. This embodiment relates to a relationship between each of active areas, which respectively correspond to divided areas and in which arrays of IGBT unit cells are disposed, and a surrounding region surrounding the active areas.

**[0089]** As shown in FIG. 20, an n⁻-base layer (a first base layer) 61 is disposed as a semiconductor active layer common to active areas D3, in which arrays of IG-

BT unit cells are disposed, and a surrounding region D4 surrounding the active areas. The $n^-$-base layer 61 has a first main surface (the top side) and a second main surface (the bottom side) opposite to each other. A plurality of p-base layers (second base layers) 62 are selectively formed in stripes by diffusion in the active areas on the top side of the $n^-$-base layer 61.

**[0090]** Two $n^+$-emitter layers (first emitter layers) 63 are selectively formed in stripes by diffusion in each of the p-base layers 62. A gate electrode 66 is formed through a gate insulating film 67 on the portion between one of the $n^+$-emitter layers 63 in one of each pair of two p-base layers 62, which are adjacent to each other, and one of the $n^+$-emitter layers 63 in the other of the two p-base layers 62. A gate electrode 66 is also formed through a gate insulating film 67 on the portion between one of the $n^+$-emitter layers 63 in each outermost p-base layer 62 and each $p^+$-ring layer 71 described later.

**[0091]** Emitter electrodes (first main electrodes) 69 are disposed in ohmic-contact with the p-base layers 62 and the $n^+$-emitter layers 63 at respective positions on the p-base layers 62. Each emitter electrode 69 is disposed on the gate electrodes 66 through an insulating protection film 68. A $p^+$-emitter layer (a second emitter layer) 65 is formed through an n-buffer layer 64 on the bottom side of the $n^-$-base layer 61. A collector electrode (a second main electrode) 70 is disposed in ohmic-contact with the $p^+$-emitter layer 65.

**[0092]** As shown in FIG. 21, $p^+$-ring layers (formed of one integral $p^+$-layer) 71 are formed in the surrounding region D4 and surround the active areas D3 in which the arrays S of IGBT unit cells are formed. Each $p^+$-ring layer 71 is electrically connected to the corresponding emitter electrode 69 through a connection electrode 69b, which is integral with the emitter electrode 69. Gate wirings 74 for supplying the gate electrodes 66 with a potential is disposed on the $p^+$-ring layers 71 through the insulating protection film 68 and surrounds the active areas D3.

**[0093]** Ring-like low-resistivity layers 73 having a resistivity lower than that of the $p^+$-ring layers 71 are respectively formed in the surface of the layers 71. Each low-resistivity layer 73 has a resistivity of from $1 \times 10^{-6}$ to $1 \times 10^{-3}$ Ω·cm and a depth of from 0.5 to 8 μm. Each low-resistivity layer 73 is disposed on the corresponding active area side relative to the center of the $p^+$-ring layer 71. Each low-resistivity layer 73 is electrically connected to the corresponding emitter electrode 69 through the connection electrode 69b, which is integral with the emitter electrode 69. Each low-resistivity layer 73 is made of a conductive material 73b buried in a trench 73a formed in the $p^+$-ring layer 71.

**[0094]** As the conductive material 73b of the low-resistivity layers 73, a metal the same as that of the emitter electrodes 69 and the connection electrodes 69b, such as aluminum (Al) used in general, is preferably used, because its contact resistance with the emitter electrodes is negligible. Where the conductive material 73b is the same as the material of the emitter electrodes 69, the low-resistivity layers 73 can be formed along with the emitter electrodes 69 in the same step by patterning a conductive film common to the emitter electrodes 69. On the other hand, where it is necessary to consider a thermal treatment to be performed in a later step, a refractory metal, such as Mo, Ti, or W, is preferably used as the conductive material 73b. Furthermore, the conductive material 73b may consist of a semiconductor, such as polycrystalline silicon, which is of a conductivity type the same as that of the $p^+$-ring layers 71 and has a carrier impurity concentration higher than that of $p^+$-ring layers 71.

**[0095]** Each low-resistivity layer 73 is disposed close to the pn junction between the $n^-$-base layer 61 and the corresponding $p^+$-ring layer 71. With this arrangement, a hole current concentrating at the $p^+$-ring layer 71 is allowed to swiftly flow into the emitter electrode 69. Each low-resistivity layer 73 is partially disposed on the corresponding p-base layers 62 side relative to the center of the $p^+$-ring layer 71. With this arrangement, a smaller amount of hole current is allowed to flow into the p-base layers 62.

**[0096]** When the IGBT is turned on, the following operation is performed. Specifically, while a positive bias is applied between the collector electrode 70 and the emitter electrodes 69 (the plus is on the collector electrode 70 side), a positive voltage (a positive bias) relative to the emitter electrodes 69 is applied to the gate electrodes 66. By doing so, n-inversion layers (not shown) are formed near the interfaces between the p-base layers 62 and the gate insulating films 67, and thus electrons are injected from the $n^+$-emitter layers 63 into the $n^-$-base layer 61. In accordance with the injection amount of the electrons, holes are injected from the $p^+$-emitter layer 65 into the $n^-$-base layer 61. As a result, the $n^-$-base layer 61 is filled with carriers and causes a conductivity modulation, and thus the resistance of the $n^-$-base layer 61 decreases to bring the IGBT into an ON-state.

**[0097]** On the other hand, when the IGBT is turned off, the following operation is performed. Specifically, in the ON-state described above, a negative bias is applied to the gate electrodes 66. By doing so, the n-inversion layers near the interfaces between the p-base layers 62 and the gate insulating films 67 disappear, and thus electrons stop being injected from the $n^+$-emitter layers 63 into the $n^-$-base layer 61. As a result, holes also stop being injected from the $p^+$-emitter layer 65 into the $n^-$-base layer 61. Then, carriers filling the $n^-$-base layer 61 are exhausted, and depletion layers expand from the junctions between the p-base layers 62 and the $n^-$-base layer 61 to bring the IGBT into an OFF-state.

**[0098]** During the turn-off operation, holes accumulated in the $n^-$-base layer 61 are exhausted through the $p^+$-ring layers 71, the low-resistivity layers 73, and the connection electrodes 69b into the emitter electrodes 69, and through the p-base layers 62 into the emitter elec-

trodes 69. Since the low-resistivity layers 73 formed in the $p^+$-ring layers 71 allow holes to easily flow, a hole current concentrates at the $p^+$-ring layers 71 preferentially to the adjacent p-base layers 62. Consequently, the adjacent p-base layers 62 are prevented from increasing the potential, thereby improving the withstanding property of the IGBT against breakdown.

**[0099]** The distance from the pn junction between each $p^+$-ring layer 71 and the $n^-$-base layer 61 to the corresponding low-resistivity layer 73 is set to be a distance at which a depletion layer extends from the pn junction into the $p^+$-ring layer 71 when the IGBT is statically-withstanding in an OFF-state. With this arrangement, the low-resistivity layer 73 can be utilized as a protection mechanism when the IGBT is supplied with an excessive voltage.

**[0100]** The relationship between the active areas D3 and the surrounding region D4 according to this embodiment is also established even where the structure of each active area D3 is replaced with that of the active area D1 shown in FIG. 15. The gate wirings 74 may further extend on a $p^+$-ring layer formed in a junction-termination region, in order to prevent gate signal delays near the junction-termination region.

(Nineteenth Embodiment)

**[0101]** FIG. 22 is a sectional view schematically showing the junction-termination region and a portion of the active area near there, of a power MOSFET according to a nineteenth embodiment of the present invention.

**[0102]** As shown in FIG. 22, an $n^-$-base layer (a first base layer) 81 is disposed as a semiconductor active layer common to the central area (corresponding to an active area) D5, in which arrays of MOSFET unit cells are disposed, and the peripheral region (corresponding to a junction-termination region) D6 surrounding the central area. The $n^-$-base layer 81 has a first main surface (the top side) and a second main surface (the bottom side) opposite to each other. A plurality of p-base layers (second base layers) 82 are selectively formed in stripes by diffusion in the central area on the top side of the $n^-$-base layer 81.

**[0103]** Two $n^+$-emitter layers (first emitter layers) 83 are selectively formed in stripes by diffusion in each of the p-base layers 82. A gate electrode 86 is formed through a gate insulating film 87 on the portion between one of the $n^+$-emitter layers 83 in one of each pair of two p-base layers 82, which are adjacent to each other, and one of the $n^+$-emitter layers 83 in the other of the two p-base layers 82. A gate electrode 86 is also formed through a gate insulating film 87 on the portion between one of the $n^+$-emitter layers 83 in each outermost p-base layer 82 and a $p^+$-ring layer 91 described later.

**[0104]** An emitter electrode (a first main electrode) 89 is disposed in ohmic-contact with the p-base layers 82 and the $n^+$-emitter layers 83 at respective positions on the p-base layers 82. The emitter electrode 89 is disposed on the gate electrodes 86 through an insulating protection film 88. An $n^+$-drain layer 99, which is of a conductivity type the same as that of the $n^-$-base layer 81 and has a carrier impurity concentration higher than that of the $n^-$-base layer 81, is formed on the bottom side of the $n^-$-base layer 81. A collector electrode (a second main electrode) 90 is disposed in ohmic-contact with the $n^+$-drain layer 99.

**[0105]** A $p^+$-ring layer 91 is formed in the junction-termination region D6 and surrounds the central area (the active area) D5 in which the arrays S of MOSFET unit cells are formed. The $p^+$-ring layer 91 is electrically connected to the emitter electrode 89 through a connection electrode 89b, which is integral with the emitter electrode 89.

**[0106]** A ring-like $n^+$-diffusion layer 94 is formed in the junction-termination region, along the peripheral edge thereof. The $n^+$-diffusion layer 94 is of a conductivity type the same as that of the $n^-$-base layer 81 and has a carrier impurity concentration higher than that of the $n^-$-base layer 81. A ring-like stopper electrode 95 in an electrically floating state is disposed on the $n^+$-diffusion layer 94. The $n^+$-diffusion layer 94 and the stopper electrode 95 constitute an equi-potential ring 96. The surface of the $n^-$-base layer 81 from the $p^+$-ring layer 91 to the $n^+$-diffusion layer 94 is covered with an insulating protection film 88.

**[0107]** A plurality of $p^+$-guard ring layers 98 are formed in the surface of the $n^-$-base layer 81 between the $p^+$-ring layer 91 and the $n^+$-diffusion layer 94. The $p^+$-guard ring layers 98 are of a conductivity type the same as that of the $p^+$-ring layer 91 and have a carrier impurity concentration higher than that of the $p^+$-ring layer 91. The distances between the $p^+$-guard ring layers 98 become gradually larger toward the peripheral edge.

**[0108]** A ring-like low-resistivity layer 93 having a resistivity lower than that of the $p^+$-ring layer 91 is formed in the surface of the layer 91. The low-resistivity layer 93 has a resistivity of from $1 \times 10^{-6}$ to $1 \times 10^{-3}$ Ω·cm and a depth of from 0.5 to 8 μm. The low-resistivity layer 93 is disposed on the active area side relative to the center of the $p^+$-ring layer 91. The low-resistivity layer 93 is electrically connected to the emitter electrode 89 through the connection electrode 89b, which is integral with the emitter electrode 89. The low-resistivity layer 93 is made of a conductive material 93b buried in a trench 93a formed in the $p^+$-ring layer 91.

**[0109]** As the conductive material 93b of the low-resistivity layer 93, a metal the same as that of the emitter electrode 89 and the connection electrode 89b, such as aluminum (Al) used in general, is preferably used, because its contact resistance with the emitter electrode is negligible. Where the conductive material 93b is the same as the material of the emitter electrode 89, the low-resistivity layer 93 can be formed along with the emitter electrode 89 in the same step by patterning a conductive film common to the emitter electrode 89. On the other hand, where it is necessary to consider a thermal treat-

ment to be performed in a later step, a refractory metal, such as Mo, Ti, or W, is preferably used as the conductive material 93b. Furthermore, the conductive material 93b may consist of a semiconductor, such as polycrystalline silicon, which is of a conductivity type the same as that of the $p^+$-ring layer 91 and has a carrier impurity concentration higher than that of $p^+$-ring layer 91.

**[0110]** The low-resistivity layer 93 is disposed close to the pn junction between the $n^-$-base layer 81 and the $p^+$-ring layer 91. With this arrangement, a hole current concentrating at the $p^+$-ring layer 91 is allowed to swiftly flow into the emitter electrode 89. The low-resistivity layer 93 is partially disposed on the p-base layers 82 side relative to the center of the $p^+$-ring layer 91. With this arrangement, a smaller amount of hole current is allowed to flow into the p-base layers 82.

**[0111]** When the power MOSFET is turned on, the following operation is performed. Specifically, while a positive bias is applied between the collector electrode 90 and the emitter electrode 89 (the plus is on the collector electrode 90 side), a positive voltage (a positive bias) relative to the emitter electrode 89 is applied to the gate electrodes 86. By doing so, n-inversion layers (not shown) are formed near the interfaces between the p-base layers 82 and the gate insulating films 87, and thus electrons are injected from the $n^+$-emitter layers 83 into the $n^-$-base layer 81. The electrons flow from the $n^-$-base layer 81 into the $n^+$-drain layer 99 to bring the MOSFET into an ON-state.

**[0112]** On the other hand, when the power MOSFET is turned off, the following operation is performed. Specifically, in the ON-state described above, a zero bias or a negative bias is applied to the gate electrodes 86. By doing so, the n-inversion layers near the interfaces between the p-base layers 82 and the gate insulating films 87 disappear, and thus electrons stop being injected from the $n^+$-emitter layers 83 into the $n^-$-base layer 81. As a result, the MOSFET is brought into an OFF-state.

**[0113]** Since the MOSFET does not generate hole currents in ON-states, there is no breakdown caused by a latched-up state due to hole current concentration. However, in an inverter circuit in which the MOSFET is generally used, parasitic diodes formed of the p-base layers 82 and the n-drain layer 99 are activated. Specifically, there is a case where a positive bias relative to the collector electrode 90 is applied to the emitter electrode 89, so that holes are injected from the p-base layers 82 and electrons are injected from the n-drain layer 99, both into the $n^-$-base layer 81, thereby bringing the parasitic diodes into an ON-state.

**[0114]** When the bias is inverted from this state, i.e., a negative bias relative to the collector electrode 90 is applied to the emitter electrode 89, holes accumulated in the $n^-$-base layer 81 are exhausted through the emitter electrode 89 out of the device. In this state, a hole current flows into the p-base layers 82 and into the $p^+$-ring layer 91. Since the low-resistivity layer 93 formed in the $p^+$-ring layer 91 allows holes to easily flow, a hole current concentrates at the $p^+$-ring layer 91 preferentially to the adjacent p-base layers 82. Consequently, the adjacent p-base layers 82 are prevented from increasing the potential, thereby improving the withstanding property of the MOSFET against breakdown.

**[0115]** The $p^+$-guard ring layers 98 cause the potential to gradually increase from the $p^+$-ring layer 91 to an equi-potential ring 96 in an OFF-state of the MOSFET. In other words, the $p^+$-guard ring layers 98 function to laterally expand an equi-potential plane in an OFF-state, thereby relaxing electrical field concentration to improve the breakdown voltage. The breakdown voltage can be controlled by changing the number of the $p^+$-guard ring layers 98.

**[0116]** The nineteenth embodiment can be combined with any one of the features described with reference to the first to eighteenth embodiments. Furthermore, the features of the first to eighteenth embodiments can be suitably combined with each other.

## Claims

1. A high breakdown voltage semiconductor device including an active area (D1, D3, D5), and a surrounding region (D2, D4, D6) surrounding the active area, **characterized by** comprising:

   a first semiconductor layer (1, 31, 61, 81) of a first conductivity type disposed as a semiconductor active layer common to the active area and the surrounding region, the first semiconductor layer having first and second main surfaces opposite to each other;
   a second semiconductor layer (2, 32, 62, 82) of a second conductivity type formed in the first main surface of the first semiconductor layer in the active area;
   a third semiconductor layer (3, 33, 63, 83) of the first conductivity type formed in a surface of the second semiconductor layer;
   a fourth semiconductor layer (5, 35, 65, 99) disposed on or in the second main surface of the first semiconductor layer in the active area;
   a gate electrode (6, 36, 66, 86) facing, through a gate insulating film, a portion of the second semiconductor layer between the first semiconductor layer and the third semiconductor layer;
   a first main electrode (9, 39, 69, 89) electrically connected to the second semiconductor layer and the third semiconductor layer;
   a second main electrode (10, 40, 70, 90) electrically connected to the fourth semiconductor layer;
   a ring layer (11, 41, 71, 91) of the second conductivity type formed in the first main surface of the first semiconductor layer and surrounding the active area at a position in the surrounding

region adjacent to the active area;
a first low-resistivity layer (13, 43, 73, 93) formed in a surface of the ring layer and having a resistivity lower than that of the ring layer; and
a connection electrode (9b, 39b, 69b, 89b) electrically connecting the first low-resistivity layer to the first main electrode.

2. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) comprises a semiconductor layer of the second conductivity type.

3. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) comprises a metal layer.

4. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) is disposed on the active area side relative to a center of the ring layer (11, 41, 71, 91).

5. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) has a resistivity of from $1 \times 10^{-6}$ to $1 \times 10^{-3}$ Ω · cm.

6. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) has a depth of from 0.5 to 8 μm.

7. A device according to claim 1, **characterized in that** the first low-resistivity layer (13, 43, 73, 93) is disposed in a trench (13a, 43a, 73a, 93a) formed in the ring layer (11, 41, 71, 91), and the first low-resistivity layer and the connection electrode (9b, 39b, 69b, 89b) comprise a conductive layer integral with the first main electrode (9, 39, 69, 89).

8. A device according to claim 1, **characterized by** further comprising a second low-resistivity layer (24) formed in a surface of the second semiconductor layer (2) and having a resistivity lower than that of the second semiconductor layer, the second low-resistivity layer being disposed in contact with the first main electrode (9) and the second and third semiconductor layers (2, 3).

9. A device according to claim 8, **characterized in that** the first and second low-resistivity layers (13, 24) consist essentially of substantially the same material.

10. A device according to claim 9, **characterized in that** the first and second low-resistivity layers (13, 24) are disposed in trenches (13a, 23) formed in the ring layer (11) and the second semiconductor layer (2), respectively.

11. A device according to claim 10, **characterized in that** the first and second low-resistivity layers (13, 24) are derived from a conductive film common to the first main electrode (9).

12. A device according to claim 11, **characterized in that** the trenches (13a, 23) accommodating the first and second low-resistivity layers (13, 24) have substantially the same depth.

13. A device according to claim 1, **characterized in that** the gate insulating film (21) comprises first and second portions (21a, 21b) formed on the second and first semiconductor layers (2, 1), respectively, the second portion being thicker than the first portion.

14. A device according to claim 1, **characterized in that** the gate insulating film (47) and the gate electrode (46) are buried in a trench (45) formed in the first semiconductor layer (31).

15. A device according to claim 14, **characterized in that** the gate electrode comprises a plurality of gate electrode portions (46) respectively buried in a plurality of trench portions (45), which are formed in the first semiconductor layer (31) with a gap therebetween, and the gap between the trench portions forms a current passageway narrow enough to increase resistance against flow of carriers of the second conductivity type from the first semiconductor layer toward the first main electrode (39) in an ON-state of the IGBT, thereby increasing ability to inject carriers of the first conductivity type from the third semiconductor layer (33) into the first semiconductor layer.

16. A device according to claim 15, **characterized by** further comprising a dummy gap portion (58) formed of a semiconductor layer portion between two of the trench portions (45) and out of contact with the first main electrode (39).

17. A device according to claim 1, **characterized in that** the fourth semiconductor layer (5, 35, 65) is of the second conductivity type.

18. A device according to claim 1, **characterized in that** the fourth semiconductor layer (99) is of the first conductivity type and has a carrier impurity concentration higher than that of the first semiconductor layer (81).

19. A device according to claim 1, **characterized in that** the active area comprises a plurality of active area portions (D3) juxtaposed on the first semiconductor layer, and the surrounding region (D4) surrounds each of the active area portions.

20. A device according to claim 1, **characterized in that** the surrounding region is a junction-termination region (D2, D6) disposed along a peripheral edge of the first semiconductor layer (1, 31, 81).

21. A device according to claim 20, **characterized by** further comprising an end layer (14, 54, 94) of the first conductivity type formed in the first main surface of the first semiconductor layer (1, 31, 81) along a peripheral edge of the first semiconductor layer, the end layer having a carrier impurity concentration higher than that of the first semiconductor layer.

22. A device according to claim 21, **characterized by** further comprising a third low-resistivity layer (26) formed in a surface of the end layer (14, 54, 94) and having a resistivity lower than that of the end layer.

23. A device according to claim 22, **characterized in that** the first and third low-resistivity layers (13, 26) consist essentially of substantially the same material.

24. A device according to claim 23, **characterized in that** the first and third low-resistivity layers (13, 26) are disposed in trenches (13a, 25) formed in the ring layer (11) and the end layer (14), respectively.

25. A device according to claim 24, **characterized in that** the first and third low-resistivity layers (13, 26) are derived from a conductive film common to the first main electrode (39).

26. A device according to claim 24, **characterized in that** the trenches (13a, 25) accommodating the first and third low-resistivity layers (13, 26) have substantially the same depth.

27. A device according to claim 20, **characterized by** further comprising a protection film (8, 19) covering the first main surface of the first semiconductor layer (1) and consisting essentially of a material selected from the group consisting of insulating materials and semi-insulating materials.

28. A device according to claim 27, **characterized by** further comprising a conductive field plate (17) extending on top of the protection film (8) in the junction-termination region, the field plate being electrically connected to the first main electrode (9).

29. A device according to claim 20, **characterized by** further comprising a RESURF layer (12) of the second conductivity type formed in the first main surface of the first semiconductor layer, disposed in contact with the ring layer, and extending in the junction-termination region, the RESURF layer having a carrier impurity concentration lower than that of the ring layer (11).

30. A device according to claim 20, **characterized by** further comprising a guard ring layer (18) of the second conductivity type formed in the first main surface of the first semiconductor layer (1) in the junction-termination region.

31. A device according to claim 30, **characterized by** further comprising a fourth low-resistivity layer (28) formed in a surface of the guard ring layer (18) and having a resistivity lower than that of the guard ring layer.

32. A device according to claim 31, **characterized in that** the first and fourth low-resistivity layers (13, 28) consist essentially of substantially the same material.

33. A device according to claim 32, **characterized in that** the first and fourth low-resistivity layers (13, 28) are disposed in trenches (13a, 27) formed in the ring layer (11) and the guard ring layer (18), respectively.

34. A device according to claim 33, **characterized in that** the first and fourth low-resistivity layers (13, 28) are derived from a conductive film common to the first main electrode (9).

35. A device according to claim 33, **characterized in that** the trenches (13a, 27) accommodating the first and fourth low-resistivity layers (13, 28) have substantially the same depth.

36. A high breakdown voltage semiconductor device including an active area (D1, D5), and a junction-termination region (D2, D6) surrounding the active area, **characterized by** comprising:

a first semiconductor layer (1, 31, 81) of a first conductivity type disposed as a semiconductor active layer common to the active area and the junction-termination region, the first semiconductor layer having first and second main surfaces opposite to each other;
a second semiconductor layer (2, 32, 82) of a second conductivity type formed in the first main surface of the first semiconductor layer in the active area;
a third semiconductor layer (3, 33, 83) of the first conductivity type formed in a surface of the second semiconductor layer;
a fourth semiconductor layer (5, 35, 99) disposed on or in the second main surface of the first semiconductor layer in the active area;
a gate electrode (6, 36, 86) facing, through a gate insulating film, a portion of the second

semiconductor layer between the first semiconductor layer and the third semiconductor layer;
a first main electrode (9, 39, 89) electrically connected to the second semiconductor layer and the third semiconductor layer;
a second main electrode (10, 40, 90) electrically connected to the fourth semiconductor layer;
a ring layer (11, 41, 91) of the second conductivity type formed in the first main surface of the first semiconductor layer and surrounding the active area at a position in the junction-termination region adjacent to the active area;
a first low-resistivity layer (13, 43, 93) formed in a surface of the ring layer and having a resistivity lower than that of the ring layer;
a connection electrode (9b, 39b, 89b) electrically connecting the first low-resistivity layer to the first main electrode;
a second low-resistivity layer (24) formed in a surface of the second semiconductor layer and having a resistivity lower than that of the second semiconductor layer, the second low-resistivity layer being disposed in contact with the first main electrode and the second and third semiconductor layers, the second low-resistivity layer consisting essentially of a material the same as that of the first low-resistivity layer;
an end layer (14) of the first conductivity type formed in the first main surface of the first semiconductor layer along a peripheral edge of the first semiconductor layer in the junction-termination region, the end layer having a carrier impurity concentration higher than that of the first semiconductor layer; and
a third low-resistivity layer (26) formed in a surface of the end layer and having a resistivity lower than that of the end layer, the third low-resistivity layer consisting essentially of a material the same as that of the first low-resistivity layer.

37. A device according to claim 36, **characterized in that** the first, second, and third low-resistivity layers (13, 24, 26) are disposed in trenches (13a, 23, 25) formed in the ring layer (11), the second semiconductor layer (2), and the end layer (14), respectively.

38. A device according to claim 37, **characterized in that** the first, second, and third low-resistivity layers (13, 24, 26) are derived from a conductive film common to the first main electrode (9).

39. A device according to claim 38, **characterized in that** the trenches (13a, 23, 25) accommodating the first, second, and third low-resistivity layers (13, 24, 26) have substantially the same depth.

40. A device according to claim 36, **characterized by** further comprising a guard ring layer (18) of the second conductivity type formed in the first main surface of the first semiconductor layer (1) in the junction-termination region, and a fourth low-resistivity layer (28) formed in a surface of the guard ring layer and having a resistivity lower than that of the guard ring layer.

41. A device according to claim 40, **characterized in that** the first to fourth low-resistivity layers (13, 24, 26, 28) consist essentially of substantially the same material.

42. A device according to claim 41, **characterized in that** the first to fourth low-resistivity layers (13, 24, 26, 28) are disposed in trenches (13a, 23, 25, 27) formed in the ring layer (11), the second semiconductor layer (2), the end layer (14), and the guard ring layer (18), respectively.

43. A device according to claim 42, **characterized in that** the first to fourth low-resistivity layers (13, 24, 26, 28) are derived from a conductive film common to the first main electrode (9).

44. A device according to claim 42, **characterized in that** the trenches (13a, 23, 25, 27) accommodating the first to fourth low-resistivity layers (13, 24, 26, 28) have substantially the same depth.

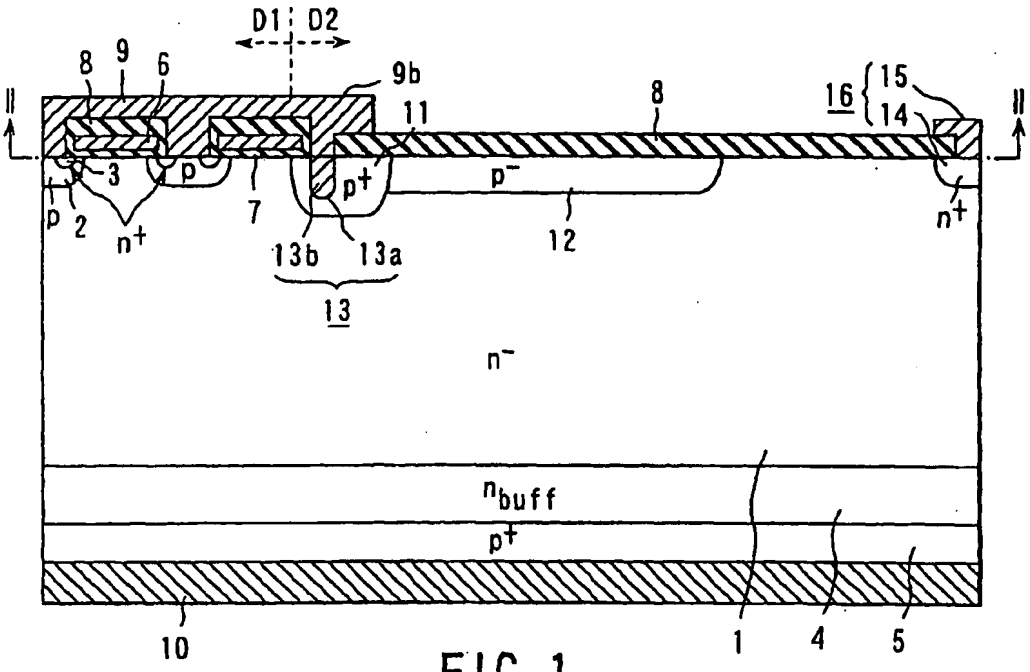



FIG. 1

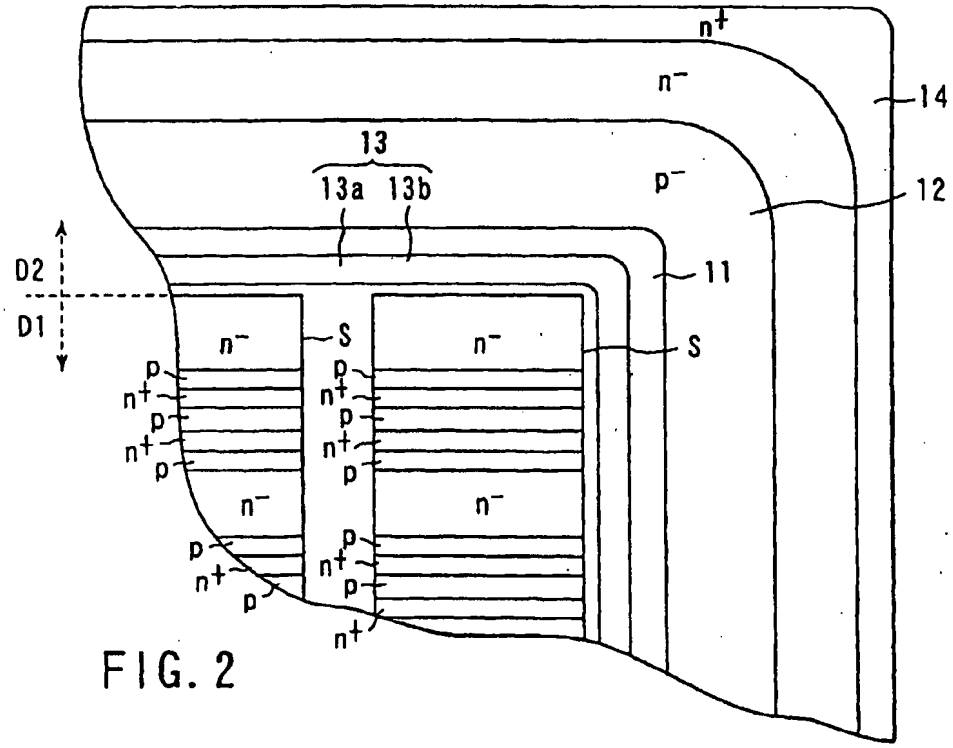



FIG. 2

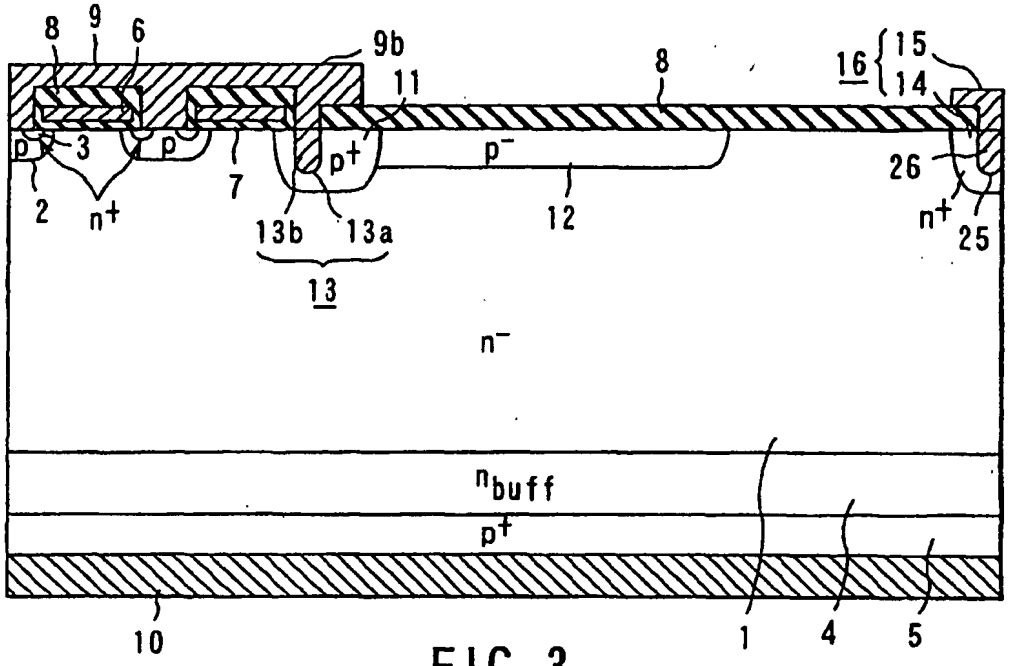



FIG. 3

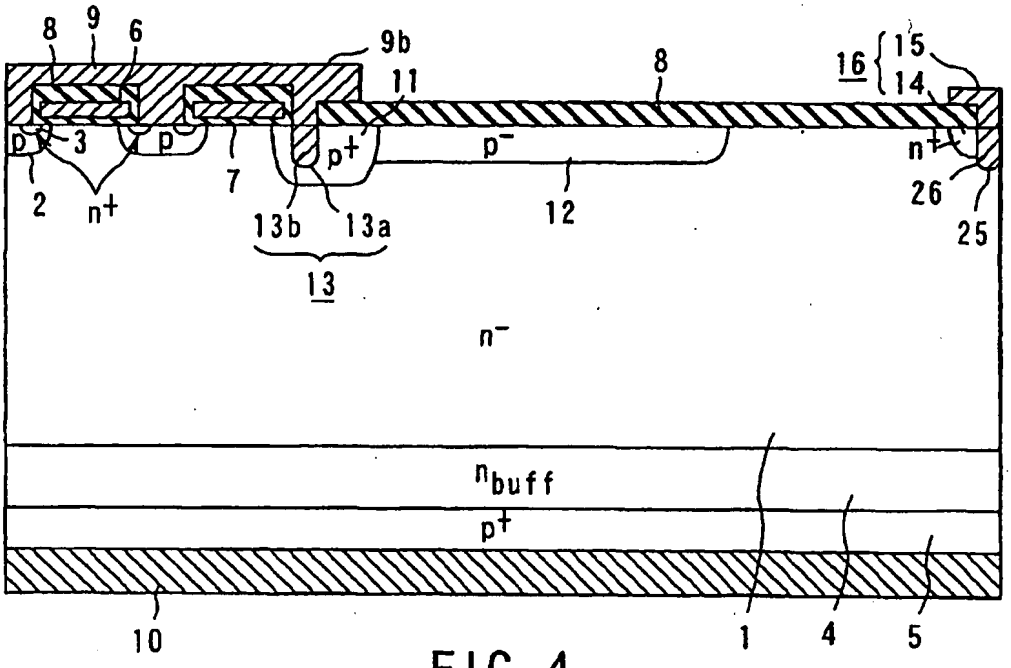



FIG. 4

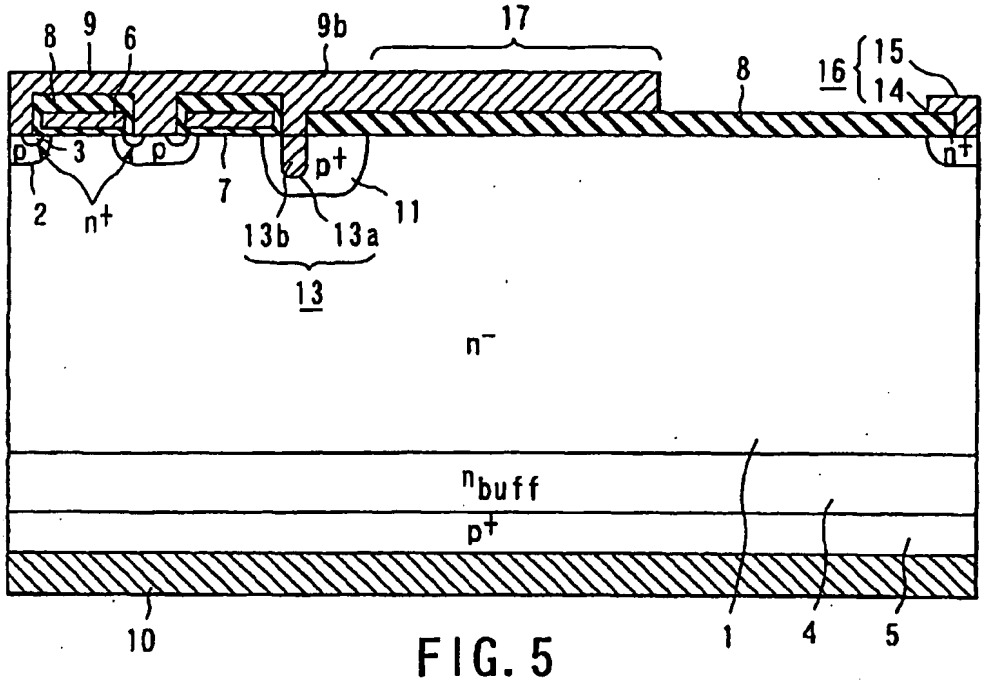



FIG. 5

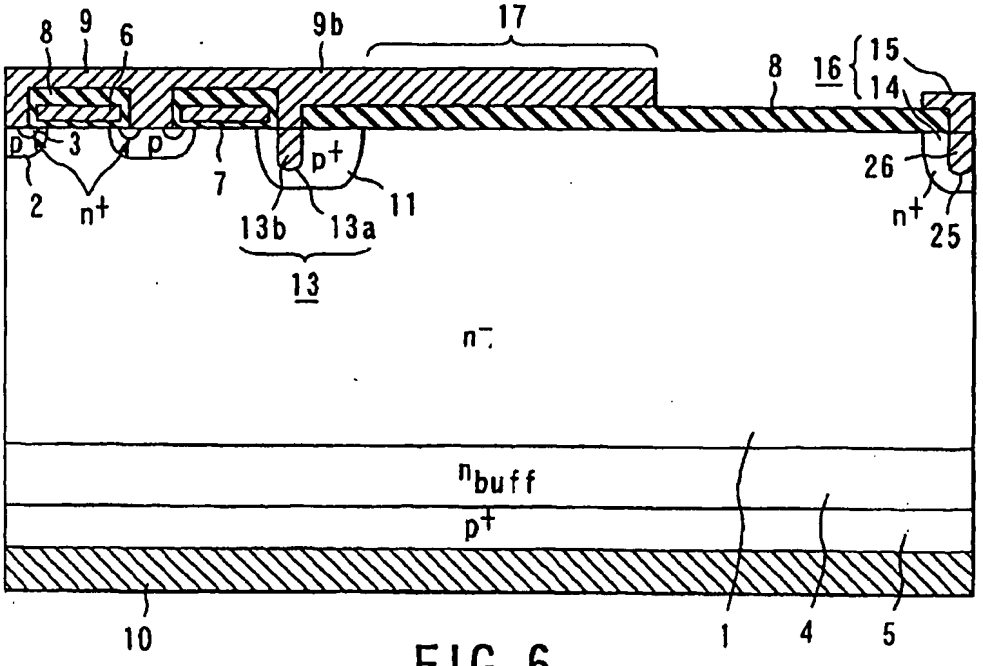
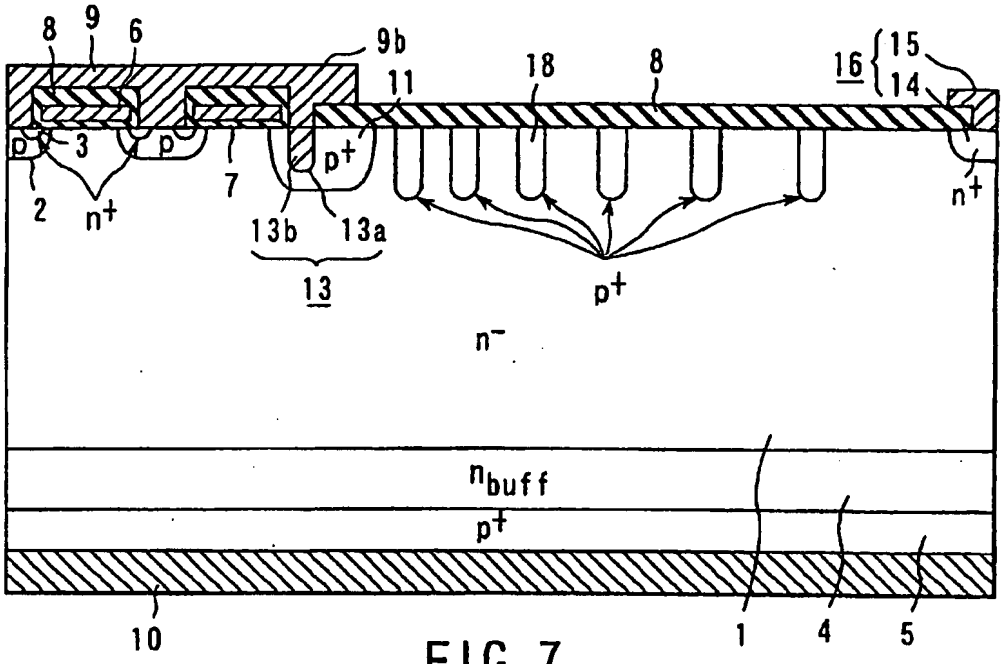



FIG. 6


8
9
6
9b
11
18
8
16
15
14
p
3
p
7
p+
2
n+
13b
13a
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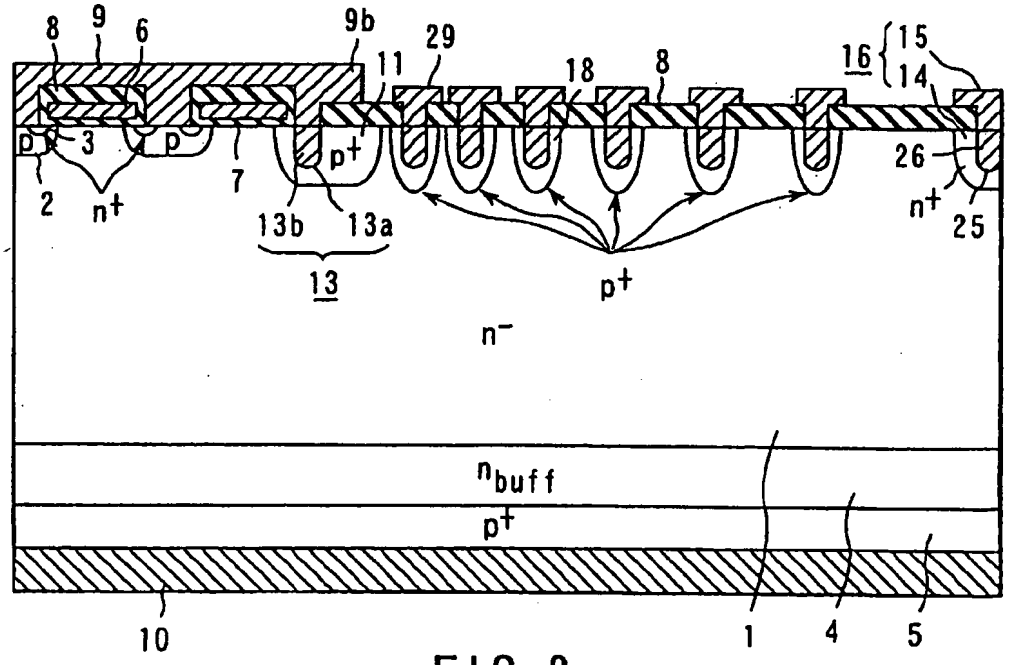
p+
n+
n−
nbuff
p+
10
1
4
5

FIG. 7


8
9
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9b
11
29
18
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16
15
14
p
3
p
7
p+
26
2
n+
n+
25
13b
13a
13
p+
n−
nbuff
p+
10
1
4
5

FIG. 8

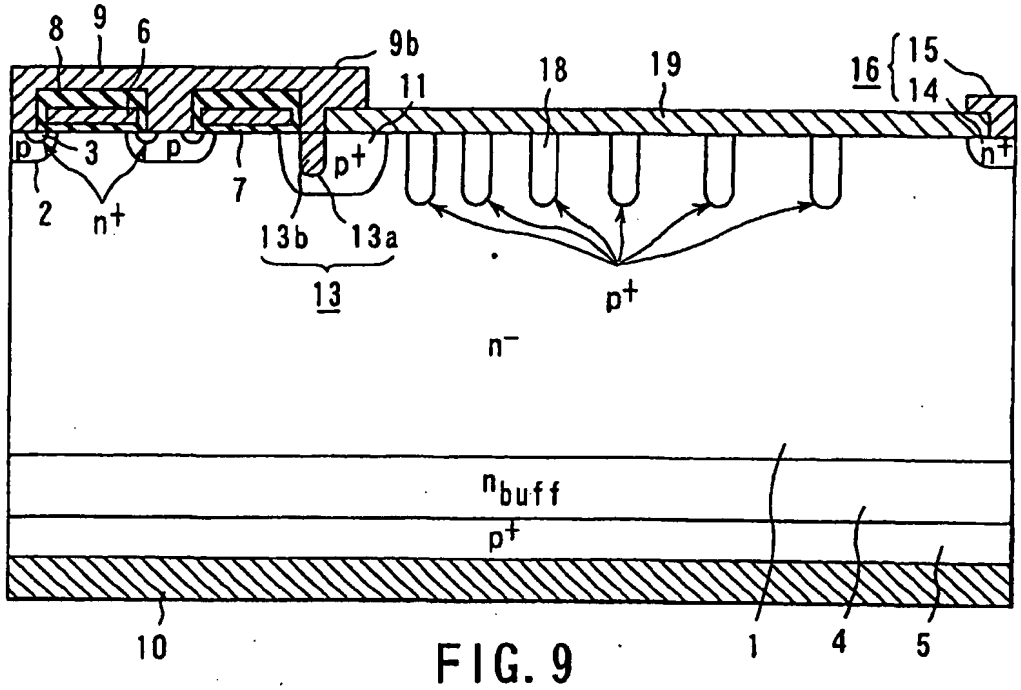



FIG. 9

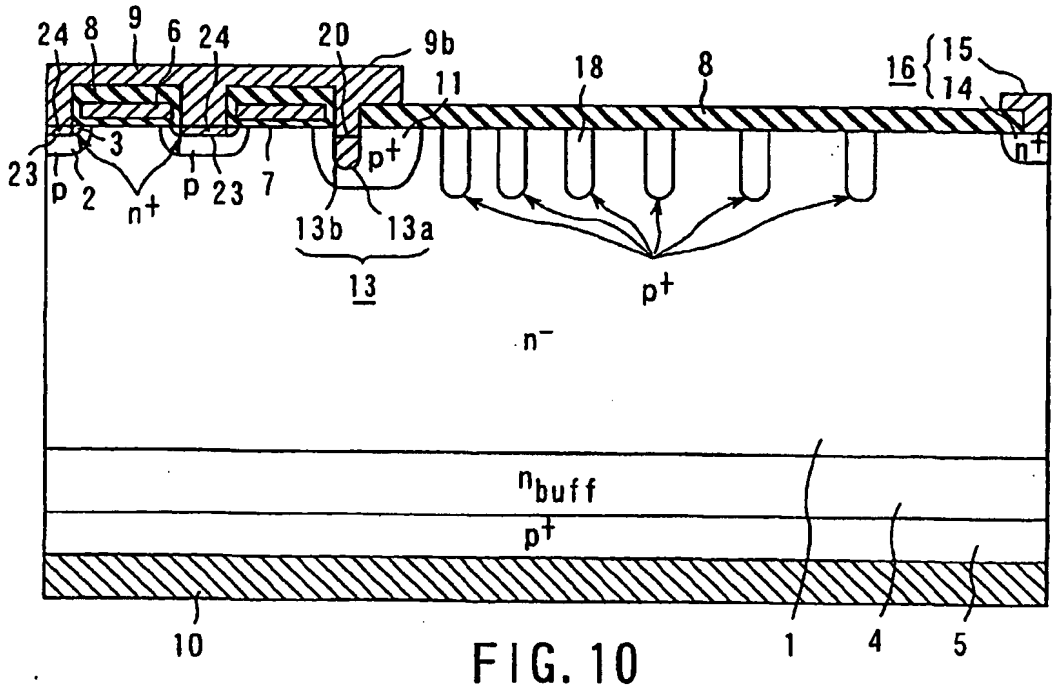
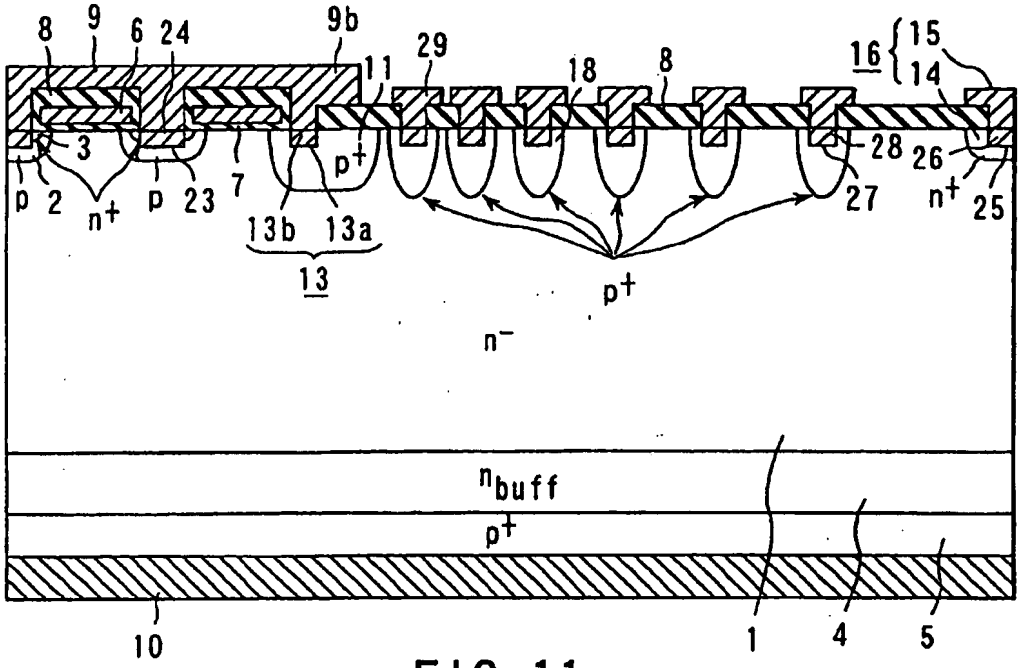



FIG. 10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24
9b
11
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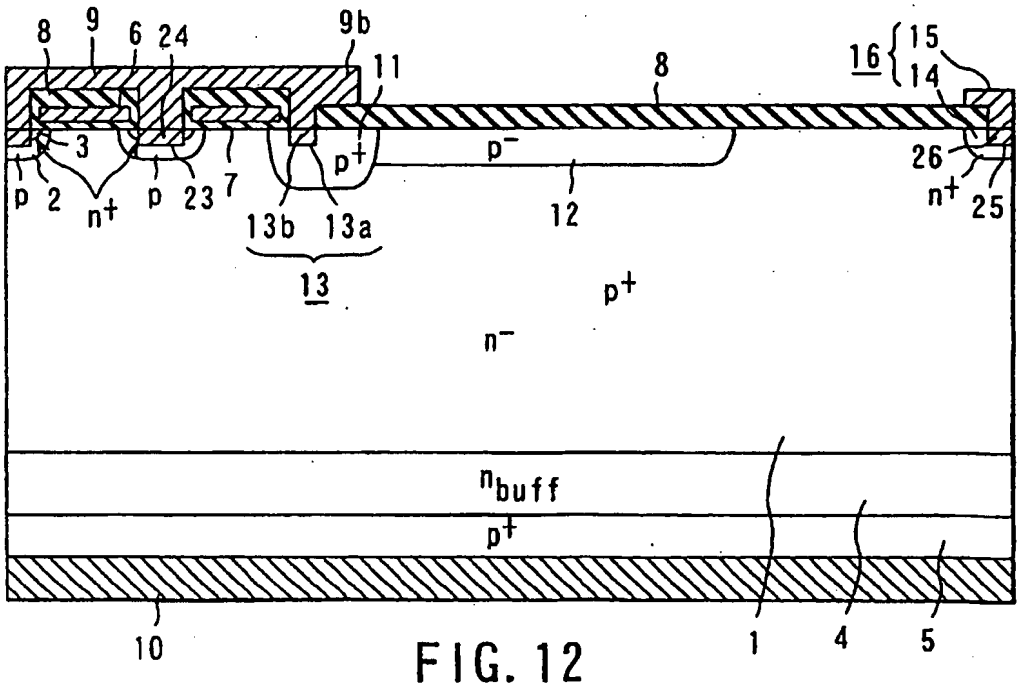
18
8
16
15
14
3
28
26
p
2
n+
p
23
7
p+
27
n+
25
13b
13a
13
p+
n−
nbuff
p+
10
1
4
5

FIG. 11


8
9
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24
9b
11
8
16
15
14
3
p−
26
p
2
n+
p
23
7
p+
12
n+
25
13b
13a
13
p+
n−
nbuff
p+
10
1
4
5

FIG. 12

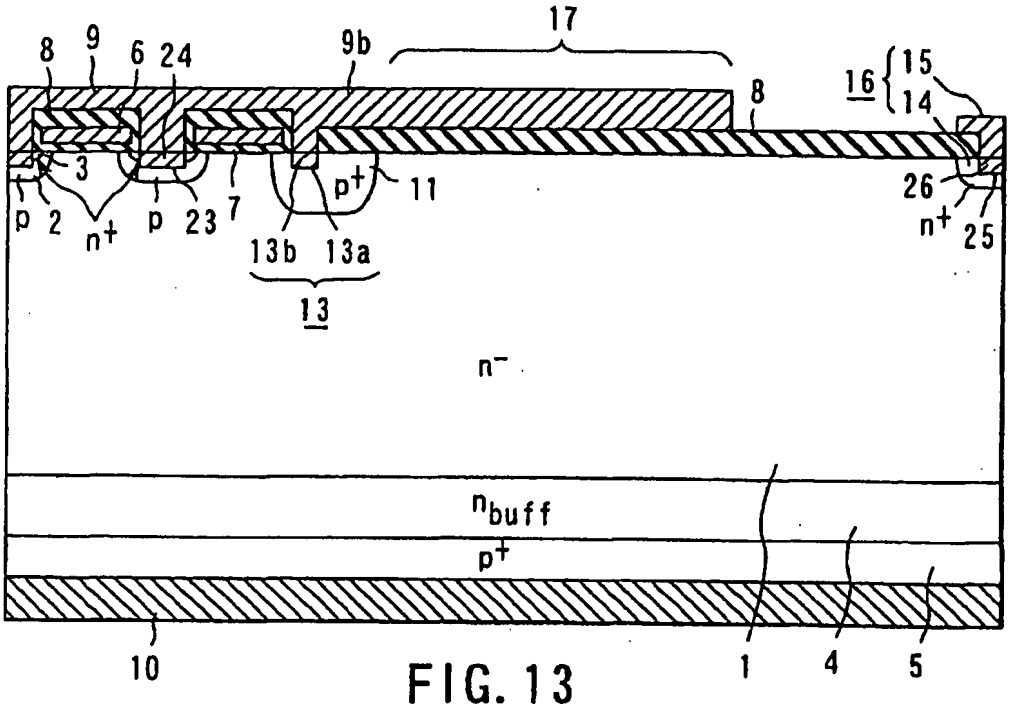



FIG. 13

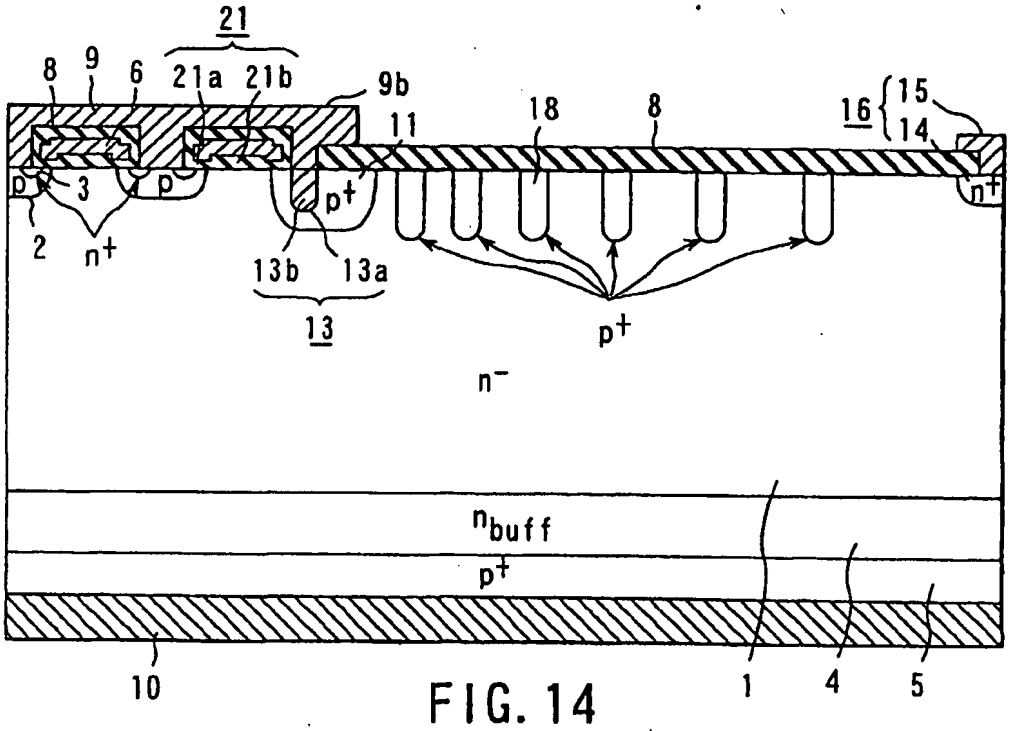
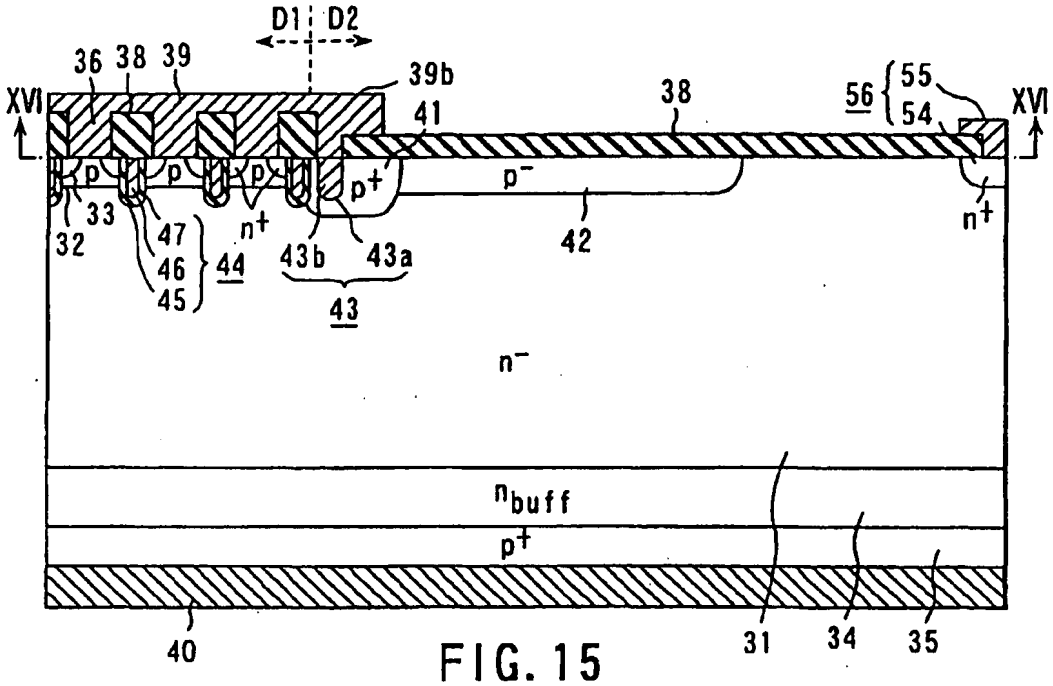



FIG. 14


D1
D2
36
38
39
39b
XVI
41
38
56
55
54
XVI
p
p
p
p
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p−
33
32
47
46
45
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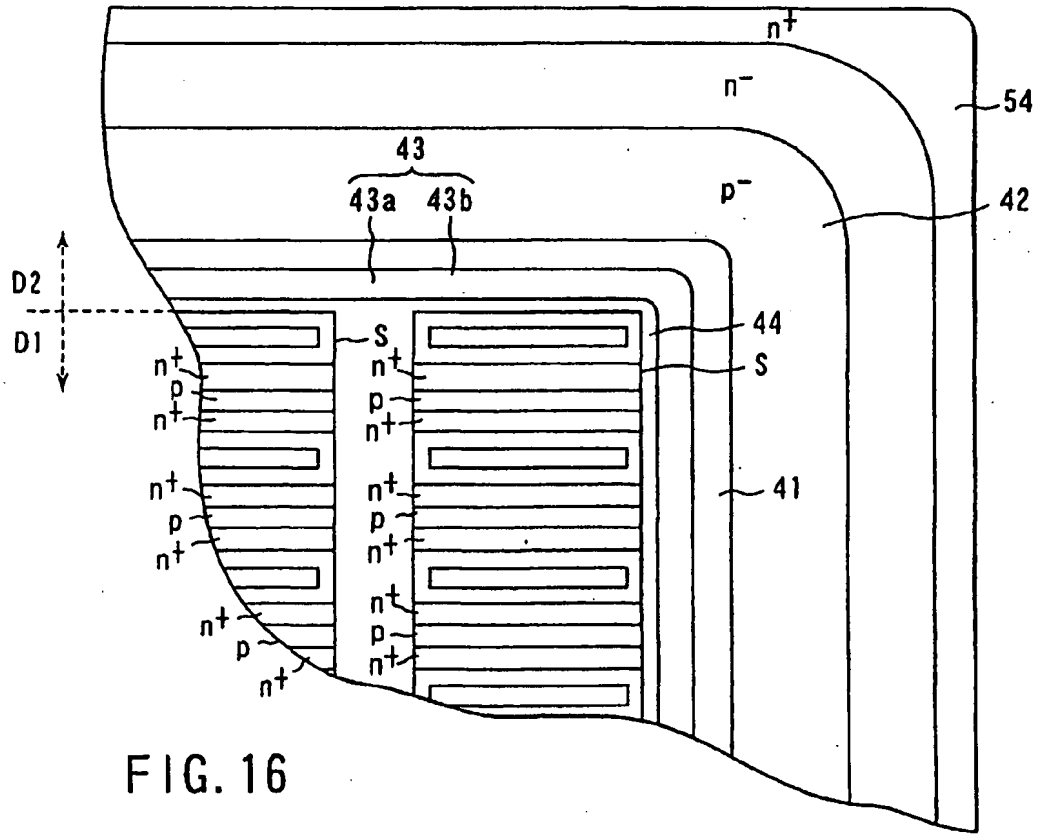
n+
43b
43a
43
42
n+
n−
nbuff
p+
40
31
34
35

FIG. 15


n+
n−
54
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43b
p−
42
D2
D1
S
44
S
n+
p
n+
41

FIG. 16

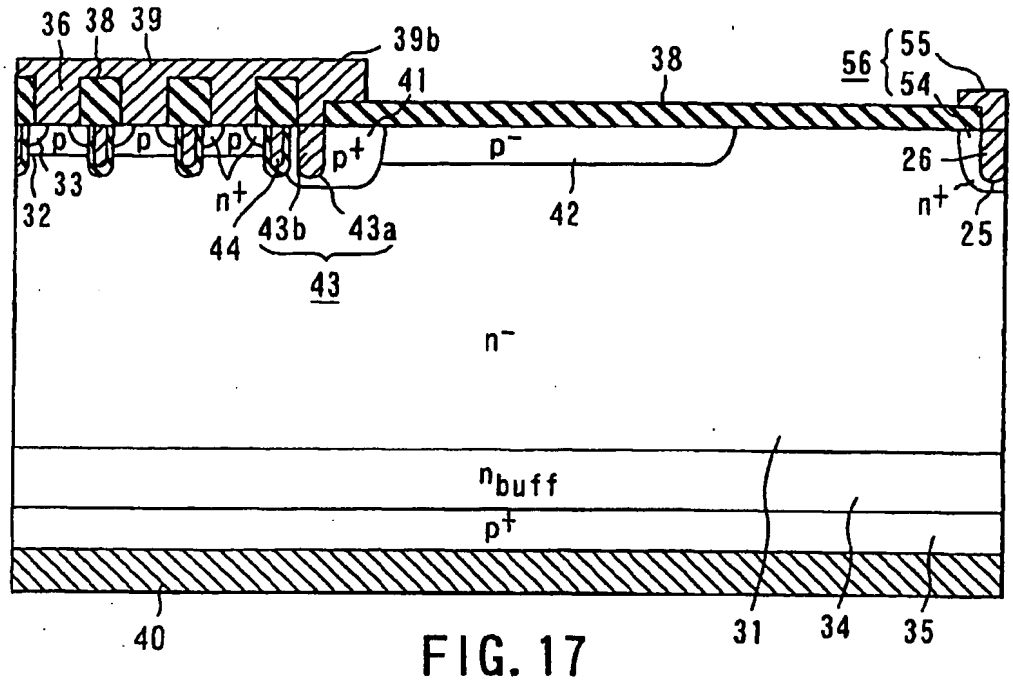


FIG. 17

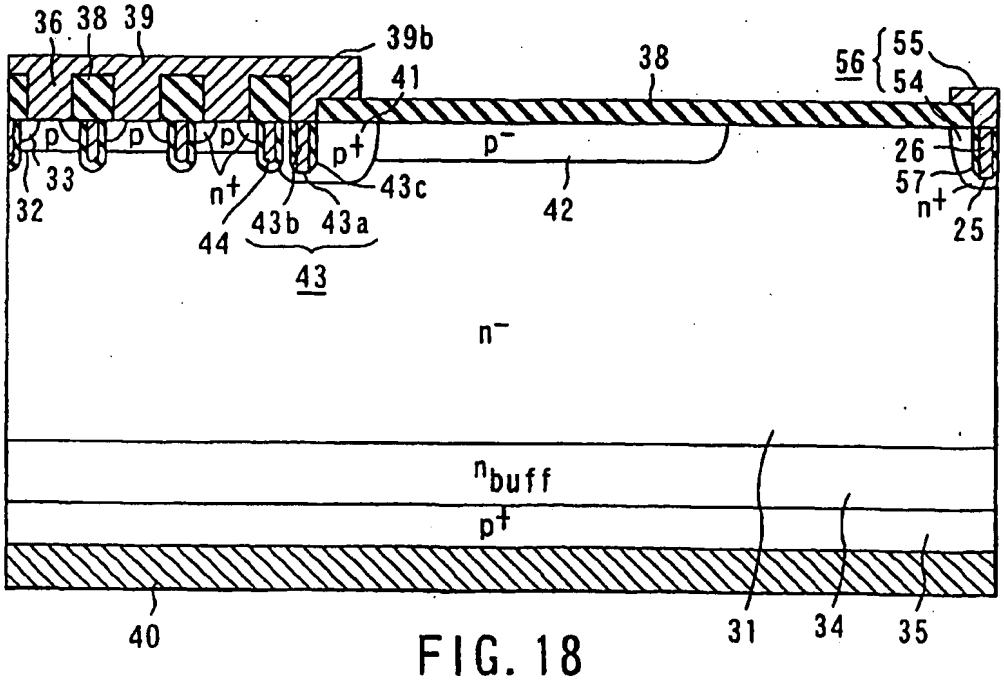


FIG. 18

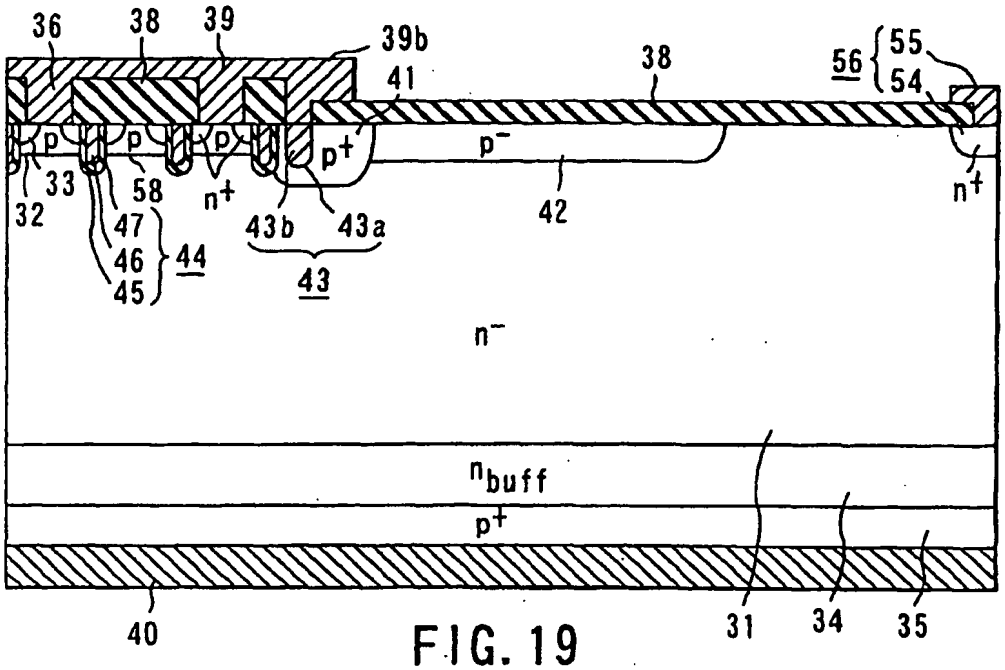


FIG. 19

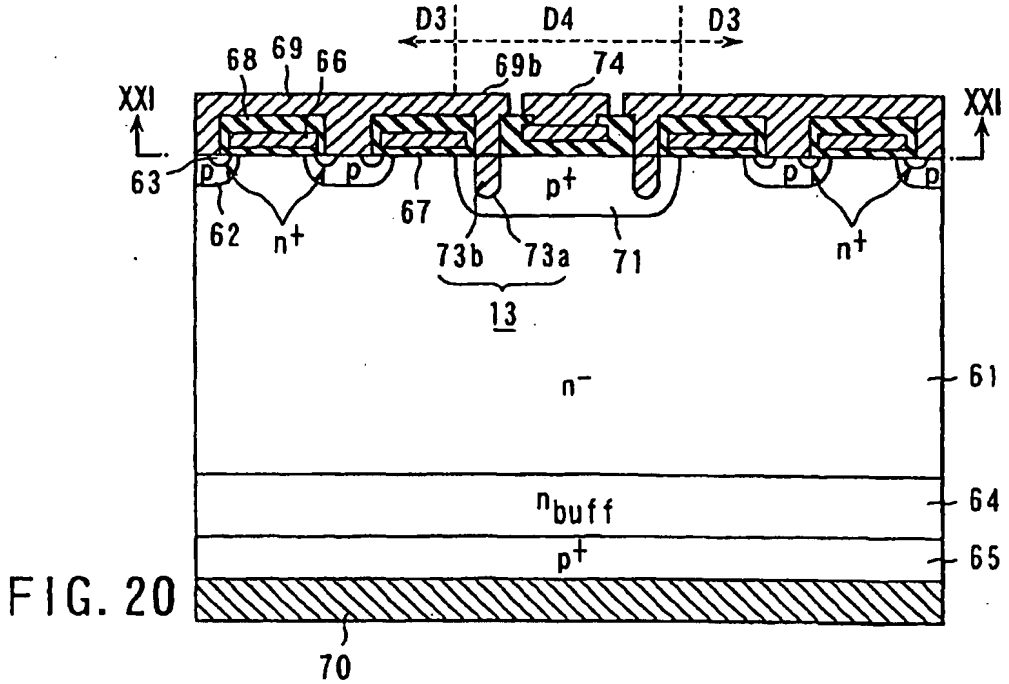


FIG. 20

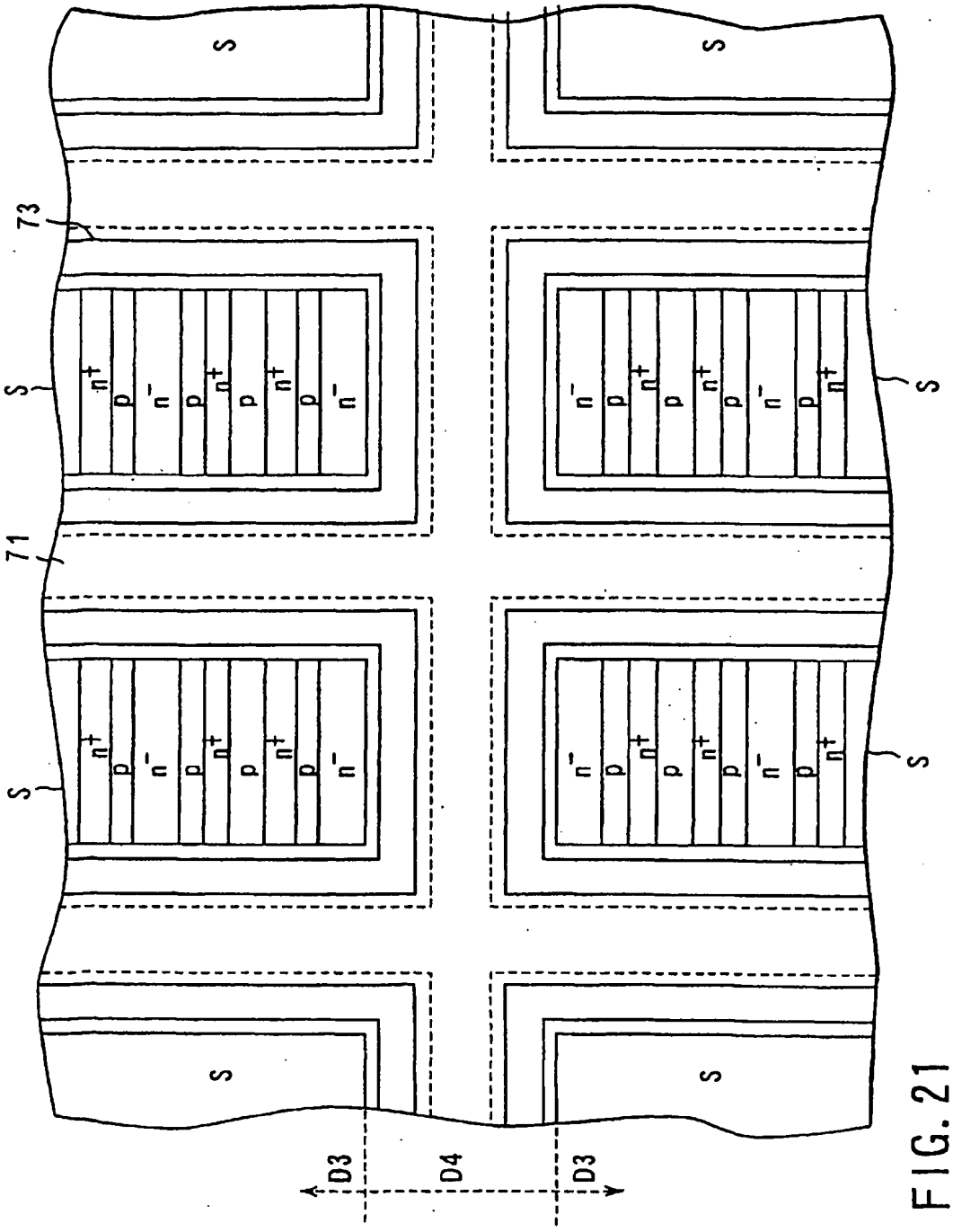


FIG. 21

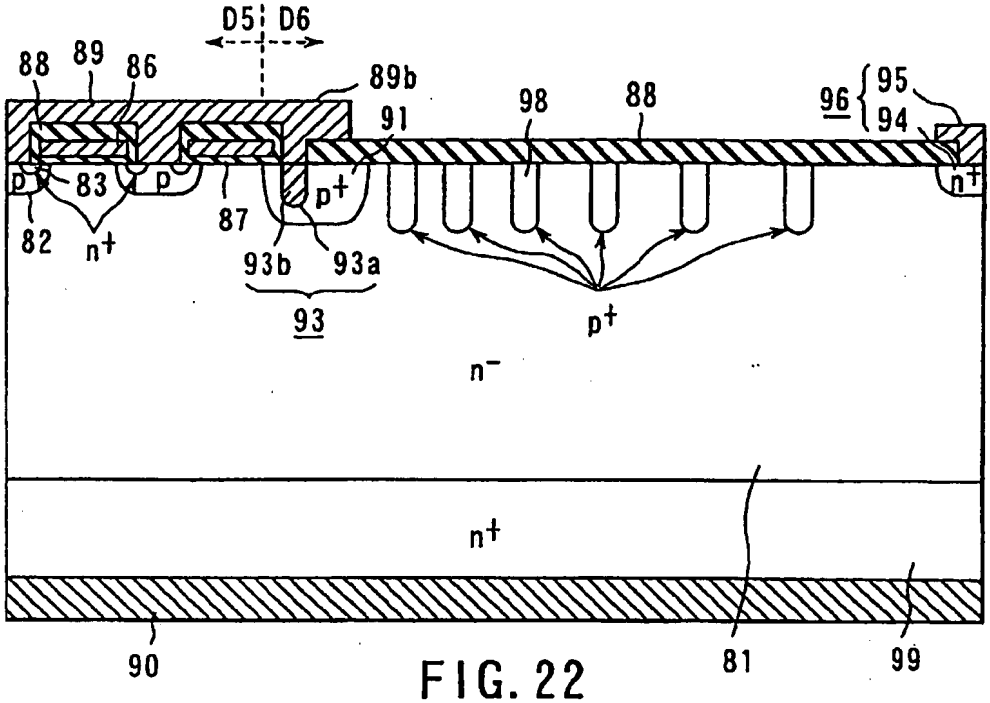


FIG. 22

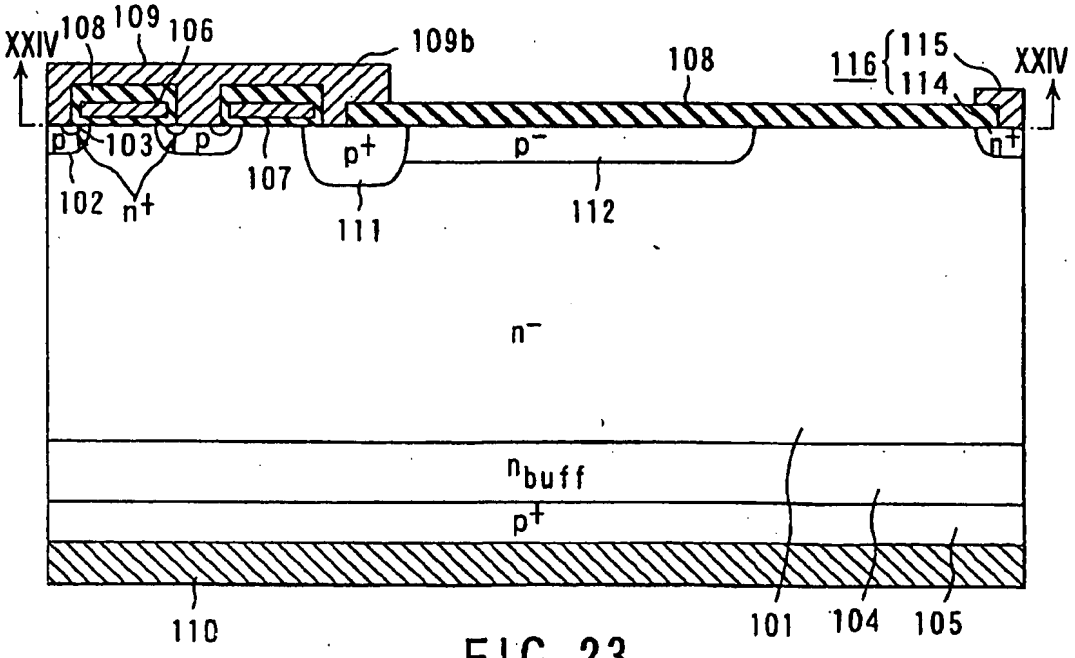


FIG. 23

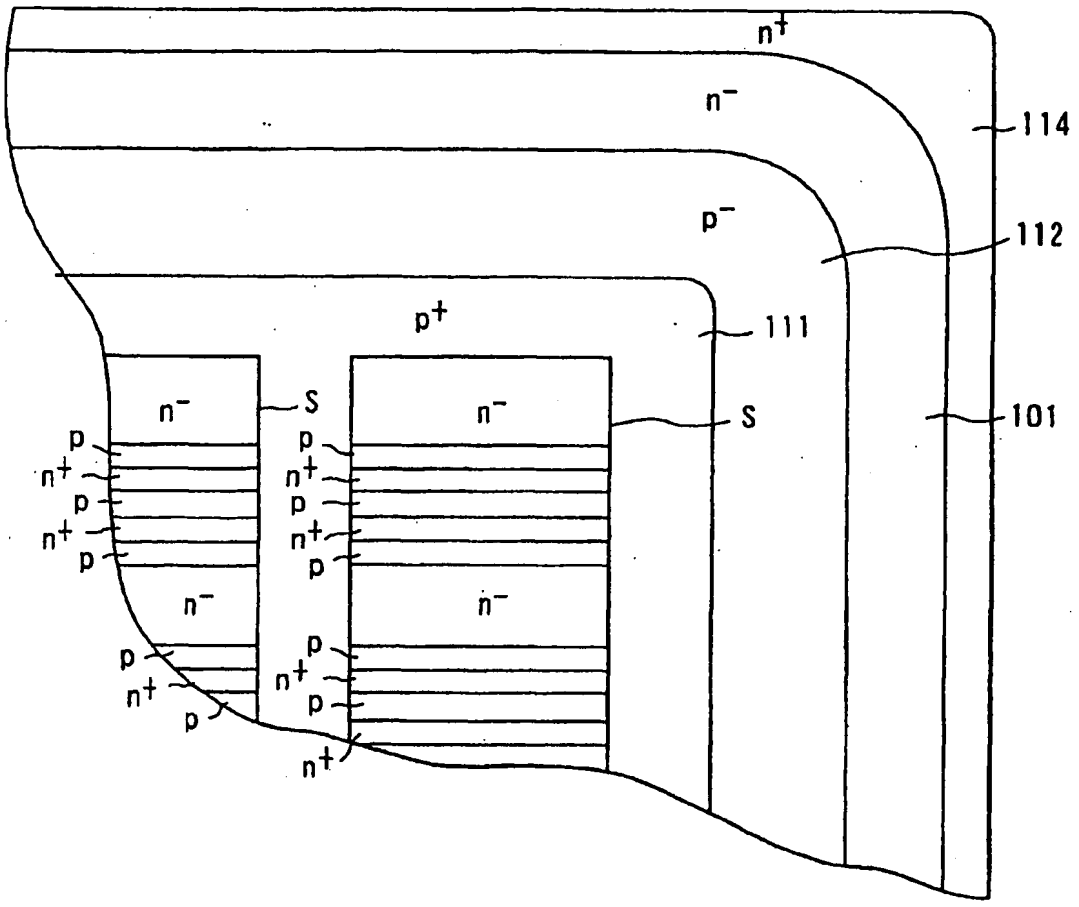


FIG. 24

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(74) Representative: **HOFFMANN - EITLE**
**Patent- und Rechtsanwälte**
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## (54) High breakdown voltage semiconductor device

(57) A high breakdown voltage semiconductor device includes an active area (D1) and a surrounding region (D2). In the active area, a second semiconductor layer (2) of a second conductivity type is formed in a first semiconductor layer (1) of a first conductivity type. A third semiconductor layer (3) of the first conductivity type is formed in the second semiconductor layer. A gate electrode (6) faces through a gate insulating film the second semiconductor layer. A first main electrode (9) is connected to the second and third semiconductor layers. A ring layer (11) of the second conductivity type surrounds the active area at a position in the surrounding region. A first low-resistivity layer (13) is formed in the ring layer and has a resistivity lower than that of the ring layer. The first low-resistivity layer is connected to the first main electrode.

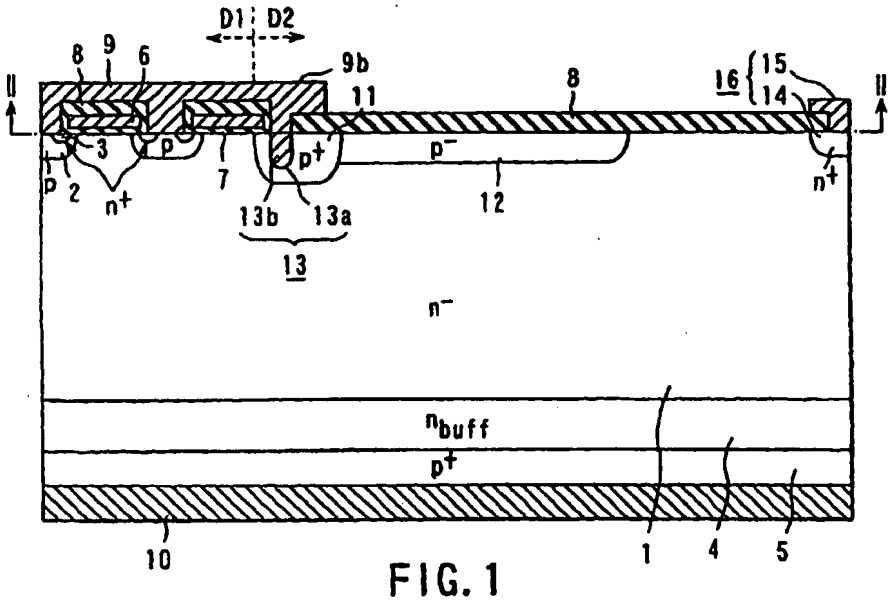


FIG. 1

EP 1 227 522 A3

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# EUROPEAN SEARCH REPORT

Application Number
EP 02 00 1150

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| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |
|---|---|---|---|
| X | US 5 169 793 A (YAMAMOTO TSUYOSHI ET AL) 8 December 1992 (1992-12-08) * column 9, line 60 - column 10, line 2; figures 1,2 * | 1-3,5,7, 17,19 | H01L29/739 H01L29/06 H01L29/10 H01L29/78 |
| Y | | 4,6,18 | |
| Y | US 5 747 853 A (LINE TRUE-LON ET AL) 5 May 1998 (1998-05-05) * abstract; figures 5,5A * | 4,18 | |
| Y | US 6 025 622 A (THUKAKOSHI THUNEO ET AL) 15 February 2000 (2000-02-15) * column 10, line 17 - line 19; figure 14 * * column 10, line 34 - line 43 * * column 1, line 51 - line 52 * | 6 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

~~The present search report has been drawn up for all claims~~

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| The Hague | 28 January 2004 | Franche, V |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 02 00 1150

## CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

## LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-7,17-19

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 02 00 1150

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-7,17-19

A high breakdown voltage semiconductor device with a low-resistivity layer in a surface of a ring layer

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2. claims: 8-12

A high breakdown voltage semiconductor device with two low resistivity layers

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3. claim: 13

A high breakdown voltage semiconductor device with a gate insulating film comprising two different portions

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4. claims: 14-16

A high breakdown voltage semiconductor device characterized in that the electrode is in a trench

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5. claims: 20-44

A high breakdown voltage semiconductor device with a junction-termination region

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## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 00 1150

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-01-2004

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